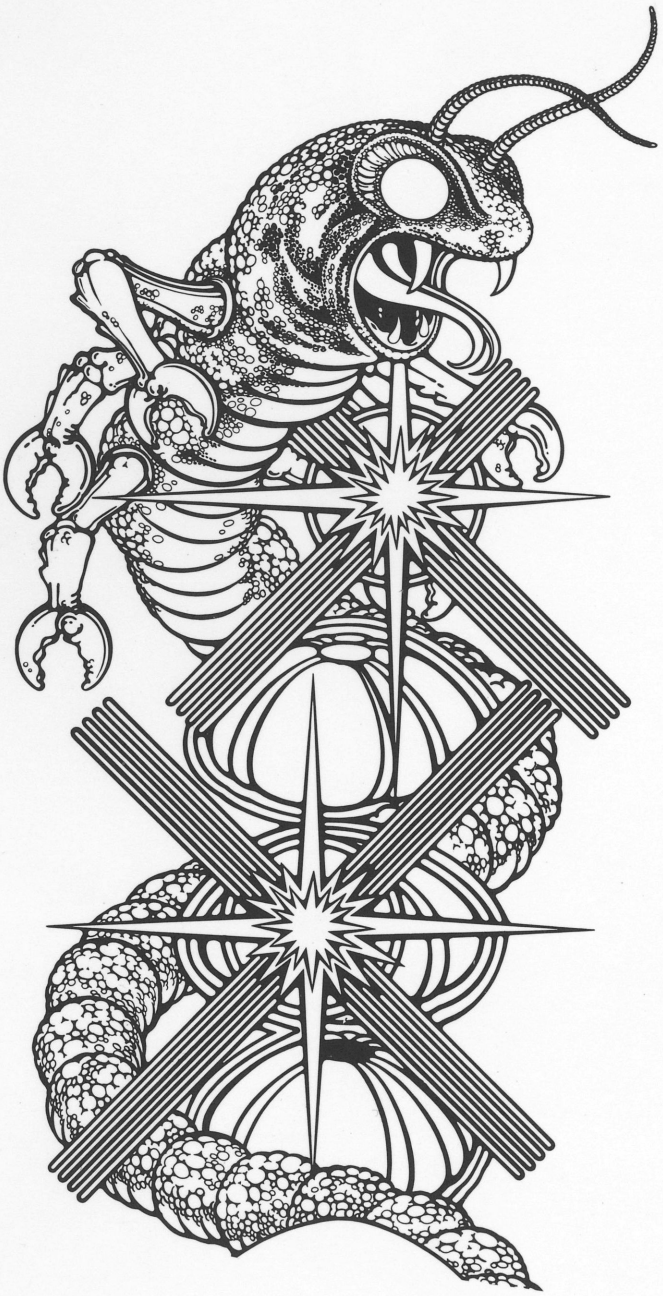
TM-192
2nd printing



Signature Analysis Guide to CENTIPEDE™

For ROM versions -002 and -003

NOTE

Before taking signatures on the Centipede™ Game PCB, examine the ROMs at locations D1, E1, F/H1, and J1 on your board. They will be marked with a part number such as 136001-208 or -308. The three digits at the end are important: they signify the version of the game program.

Your PCB may have either all -200 series or -300 series ROMs (you can not mix the series in these four ROMs).

The signatures are different for these two series of ROMs. Therefore, refer to the appropriate column under **Signatures Should Be** when taking signatures.

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Signature Analysis for Centipede™

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1. Set-Up for Signature Analysis

A. CAT Box Preliminary Set-Up

1. Remove:
   - The electrical power from the game.
   - The wiring harness from the game PCB.
   - The game PCB from the cabinet.
   - The MPU chip C2 from the game PCB.

2. Connect:
   - The extender cables to the game PCB and the wiring harness.
   - Pins 37 to 39 on the MPU socket with a piece of 28 AWG wire.
   - The CAT Box flex cable to the game PCB test edge connector.

B. Signature Analysis Procedure

1. Connect the three BNC to E-Z clip cables (supplied with the CAT Box) to the SIGNATURE ANALYSIS CONTROL START, STOP, and CLOCK jacks on the CAT Box.

2. Attach the three black E-Z clips to a ground loop on the Centipede™ game PCB.

3. Attach the CAT Box data probe to the DATA jack on the CAT Box.

4. The colored E-Z clips on the cables will be moved about for each group of signatures to be taken. The set-up for each group of signatures is located on the schematic sheet near the device to be checked. The signatures are located on or near the signal point on the schematic.

5. Set the CAT Box switches as follows:
   a. TESTER MODE: SIG
   b. TESTER SELF-TEST: OFF
   c. PULSE MODE: LATCHED
   d. START: As indicated
   e. STOP: As indicated
   f. CLOCK: As indicated

6. Power up the game board and the CAT Box.

2. Checking Address Lines

A. CAT Box Settings for Address Test

Probe	*Trigger*	*IC-Pin*	*Test Pt.*
Start	⌐	C2-25	
Stop	⌐	C2-25	
Clock	⌐	C2-39	Φ2

B. Signatures

Logic Probe on IC-Pin	*Signal Name*	*Signature Should Be*
C1-12	AB0	UUUU
C1-14	AB1	5555
C1-16	AB2	CCCC
C1-18	AB3	7F7F
C1-9	AB4	5H21
C1-7	AB5	0AFA
C1-5	AB6	UPFH
C1-3	AB7	52F8
B1-12	AB8	HC89
B1-14	AB9	2H70
B1-16	AB10	HPP0
B1-5	AB11	1293
B1-3	AB12	HAP7
C2-23	A13	3C96
C2-24	A14	3827
C2-25	A15	755U

3. Checking Address Decoder

A. CAT Box Settings for Address Decoder Test

Probe	*Trigger*	*IC-Pin*	*Test Pt.*
Start		C2-25	
Stop		C2-25	
Clock		C2-39	Φ2

B. Signatures

Logic Probe on IC-Pin	*Signal Name*	*Signature Should Be*
K3-10		3C97
J3-8	$\overline{\text{ROM}}$	3C97
J2-9	$\overline{\text{ROM3}}$	51U7
J2-10	$\overline{\text{ROM2}}$	2960
J2-11	$\overline{\text{ROM1}}$	5P33
J2-12	$\overline{\text{ROM0}}$	1H32
H3-11		A8H2
H3-10		C5P1
H3-9		U550
H3-7		9UC6
H3-6		0UA5
H3-5	$\overline{\text{POKEY}}$	F733
H3-4		4231
H3-3	$\overline{\text{SWRD}}$	3580
H3-2	$\overline{\text{PF}}$	4P5C
H3-1	$\overline{\text{RAM0}}$	A00H
J3-11		F6HP
C5-8		F97A
C4-6	$\overline{\text{EA READ}}$	0099
C4-5	$\overline{\text{EA CONTROL}}$	U08U
C4-4	$\overline{\text{EA ADDR}}$	HF7A
E3-3	$\overline{\text{IN0}}$	0294
K3-12		5554
E3-6	$\overline{\text{IN1}}$	40A4
E3-8	$\overline{\text{PFRAMRD}}$	4P5C

For the following four tests, ground J2, pin 1:

J2-7	$\overline{\text{PFWR3}}$	11U6
J2-6	$\overline{\text{PFWR2}}$	1C3F
J2-5	$\overline{\text{PFWR1}}$	4FH7
J2-4	$\overline{\text{PFWR0}}$	461F

4. Checking ROM and Data Lines

A. CAT Box Settings for ROM0 Test (I.C. D1)

Probe	*Trigger*	*IC-Pin*	*Test Pt.*
Start		D1-20	$\overline{\text{ROM0}}$
Stop		D1-20	$\overline{\text{ROM0}}$
Clock		C2-39	Φ2

To obtain stable signatures from ROM0, it may be necessary to install a 1000 pf capacitor from K3-11 to ground.

B. Signatures

Logic Probe on IC-Pin	*Signal Name*	*-200 ROMs: Signature Should Be*	*-300 ROMs: Signature Should Be*
D1-9	DB0	5AF2	8H07
D1-10	DB1	3276	7916
D1-11	DB2	48UH	7052
D1-13	DB3	P316	H3FH
D1-14	DB4	PF7A	H6F1
D1-15	DB5	H973	1322
D1-16	DB6	3F34	U577
D1-17	DB7	U638	F189

C. CAT Box Settings for ROM1 Test (I.C. E1)

Probe	*Trigger*	*IC-Pin*	*Test Pt.*
Start		E1-20	$\overline{\text{ROM1}}$
Stop		E1-20	$\overline{\text{ROM1}}$
Clock		C2-39	Φ2

To obtain stable signatures from *ROM1,* it may be necessary to install a 1000 pf capacitor from K3-11 to ground.

D. Signatures

Logic Probe on IC-Pin	*Signal Name*	*-200 ROMs: Signature Should Be*	*-300 ROMs: Signature Should Be*
E1-9	DB0	13PH	2956
E1-10	DB1	C4P5	18F6
E1-11	DB2	11F3	F829
E1-13	DB3	098P	6200
E1-14	DB4	5H24	47C0
E1-15	DB5	0548	F341
E1-16	DB6	33P7	67FP
E1-17	DB7	80AA	8UF5

E. CAT Box Settings for Address Decoder Test (I.C. F/H1)

Probe	*Trigger*	*IC-Pin*	*Test Pt.*
Start		F/H1-20	$\overline{\text{ROM2}}$
Stop		F/H1-20	$\overline{\text{ROM2}}$
Clock		C2-39	Φ2

F. Signatures

Logic Probe on IC-Pin	*Signal Name*	*-200 ROMs: Signature Should Be*	*-300 ROMs: Signature Should Be*
F/H1-9	DB0	CU62	77C1
F/H1-10	DB1	9553	04CC
F/H1-11	DB2	7756	11F0
F/H1-13	DB3	A7CF	6UC2
F/H1-14	DB4	6081	1300
F/H1-15	DB5	5HAC	6572
F/H1-16	DB6	6U43	U047
F/H1-17	DB7	F83H	9U68

G. CAT Box Settings for ROM3 Test (I.C. J1)

Probe	*Trigger*	*IC-Pin*	*Test Pt.*
Start		J1-20	$\overline{\text{ROM3}}$
Stop		J1-20	$\overline{\text{ROM3}}$
Clock		C2-39	Φ2

H. Signatures

Logic Probe on IC-Pin	*Signal Name*	*-200 ROMs: Signature Should Be*	*-300 ROMs: Signature Should Be*
J1-9	DB0	476H	75CU
J1-10	DB1	2A2C	3FFA
J1-11	DB2	2337	F717
J1-13	DB3	FP07	H5U0
J1-14	DB4	A9AF	959U
J1-15	DB5	12HA	5050
J1-16	DB6	2367	C439
J1-17	DB7	8P82	HF82

5. Checking Horizontal Sync (Synchronizer)

A. CAT Box Settings for P2 Counter Test

Probe	*Trigger*	*IC-Pin*
Start		P2-11
Stop		P2-11
Clock		P2-2

B. Signatures

Logic Probe on IC-Pin	*Signal Name*	*Signature Should Be*
P2-15	—	0102
P2-14	6MHz	55H1
P2-13	1H	334U
P2-12	2H	0U16
K4-11	—	0102
N1-6	$\overline{\text{6MHz}}$	ACA2

C. CAT Box Settings for N2 Counter Test

Probe	*Trigger*	*IC-Pin*
Start		N2-11
Stop		N2-11
Clock		P2-2

D. Signatures

Logic Probe on IC-Pin	*Signal Name*	*Signature Should Be*
N2-15	—	C3F2
N2-14	8H	7P25
N2-13	16H	85PA
N2-12	32H	77F7

E. CAT Box Settings for M2 Counter Test

Probe	*Trigger*	*IC-Pin*
Start		M2-13
Stop		M2-13
Clock		P2-2

F. Signatures

Logic Probe on IC-Pin	*Signal Name*	*Signature Should Be*
M2-15	—	FH5F
M2-14	128H	4596
N1-10	—	CC34
M3-8	—	1979
M3-5	HSYNC	P77U
M3-6	$\overline{\text{HSYNC}}$	309C
M4-3	256H2D	2633
M4-15	256HD	A829
M4-14	$\overline{\text{256HD}}$	7UFH
N1-4	$\overline{\text{4H}}$	H93H
L4-3	COLOREN	A829
L4-2	—	7UFH
L8-11	$\overline{\text{HBLANK}}$	8304
D4-8	—	24U5

6. Checking Vertical Sync (Synchronizer)

A. CAT Box Settings for P3 Counter Test

Probe	*Trigger*	*IC-Pin*
Start		P3-11
Stop		P3-11
Clock		P2-2

B. Signatures

Logic Probe on IC-Pin	*Signal Name*	*Signature Should Be*
P3-15	—	H7P4
P3-14	1V	3F3U
P3-13	2V	UUCC
P3-12	4V	2A42

C. CAT Box Settings for N3 Counter Test

Probe	*Trigger*	*IC-Pin*
Start		N3-11
Stop		N3-11
Clock		P2-2

D. Signatures

Logic Probe on IC-Pin	*Signal Name*	*Signature Should Be*
N3-14	16V	239F
N3-13	32V	6U0H
N3-12	64V	U047
P4-9	—	F91U
P4-10	—	5890
P4-11	—	108A
P4-12	—	FUU7
N4-10	VBLANK	9H7H
N4-11	$\overline{\text{VBLANK}}$	C697
N4-6	$\overline{\text{VRESET}}$	94FP
N4-2	VSYNC	F5U6
N4-3	$\overline{\text{VSYNC}}$	PP1F
M4-10	$\overline{\text{VBLANKD}}$	8F15