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GAUNTLET™

Schematic Package Supplement to the Gauntlet™ Operators Manual

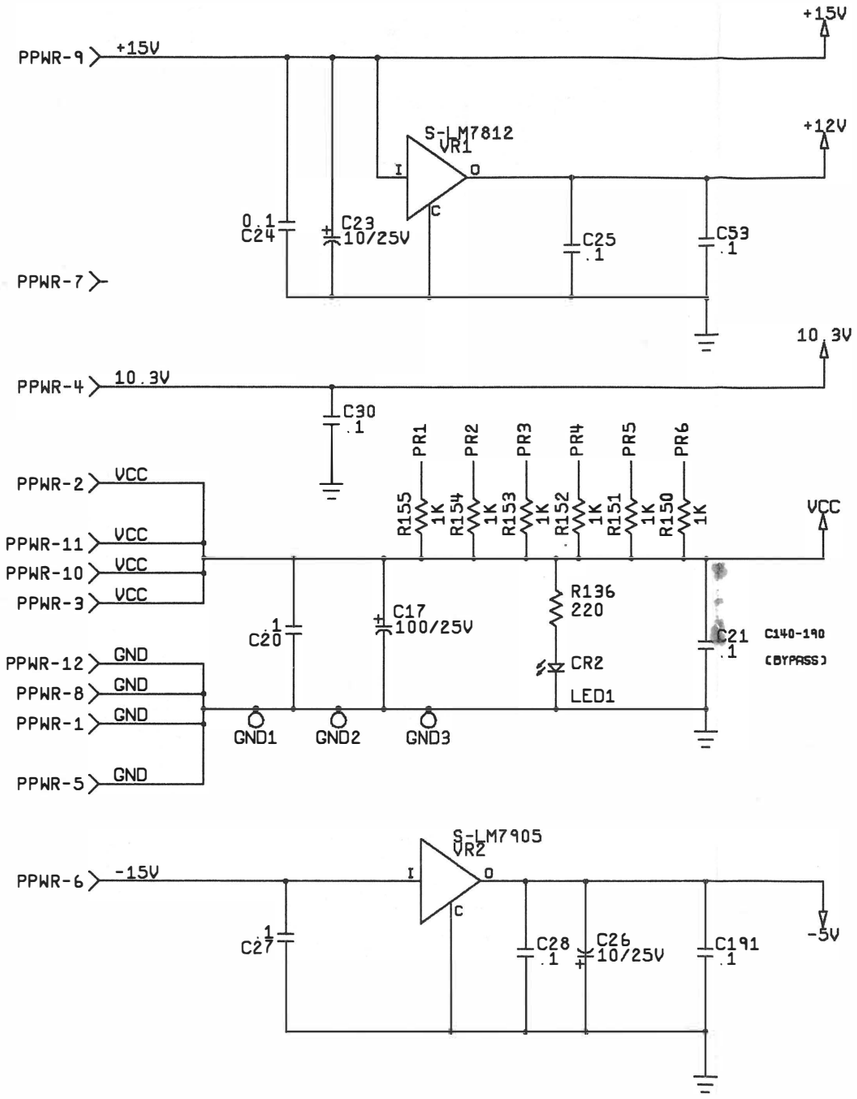
NOTE
This staple temporarily holds the schematic package together. Remove the staple before using these schematics.



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NOTE
In the schematics printed on Sheets 1–16 a slash (/) in front of a signal name indicates an active low signal. In the signal name glossary (printed at the end of this schematic package) these signals are overscored, e.g., $\overline{\text{COMPSYNC}}$.



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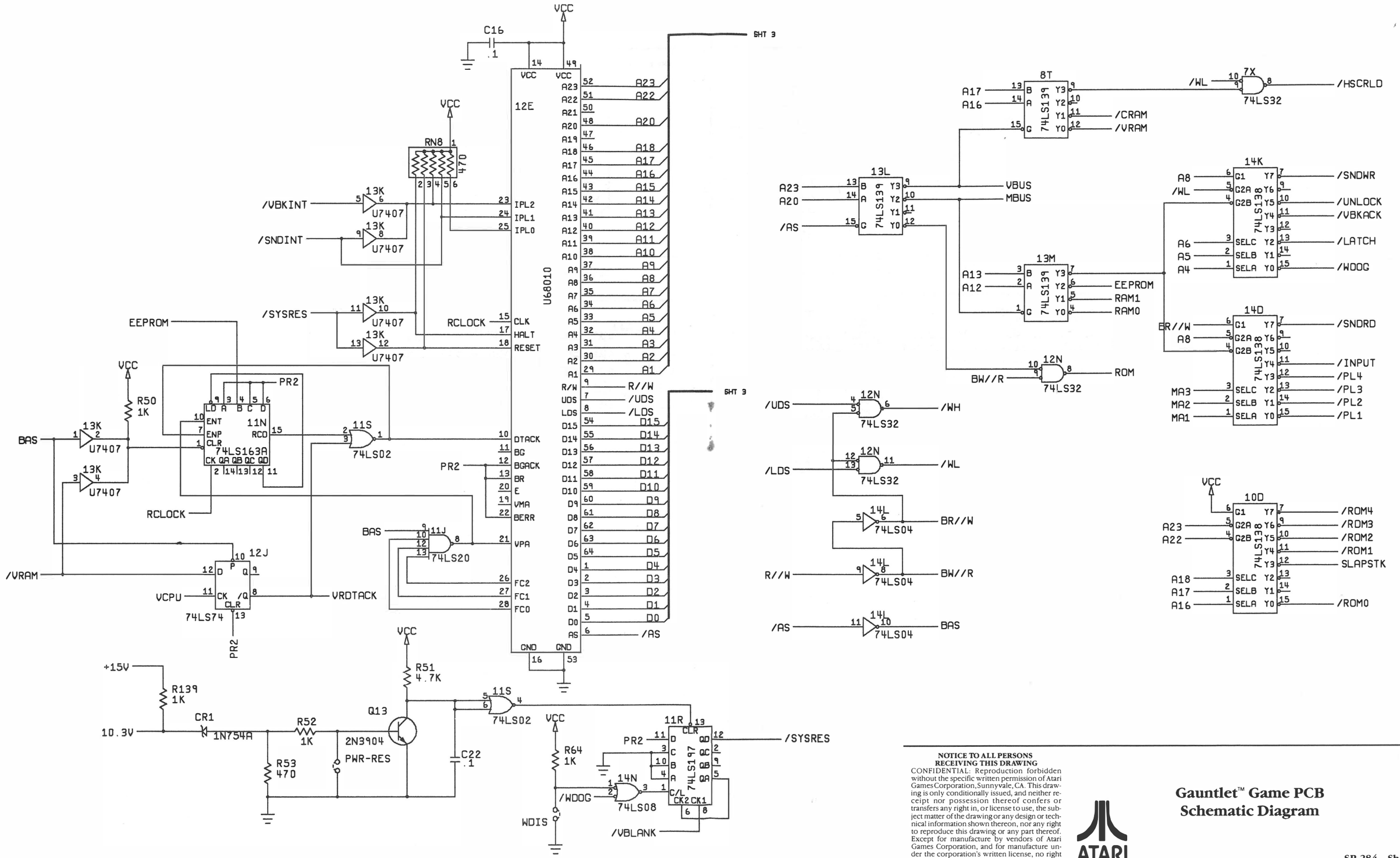
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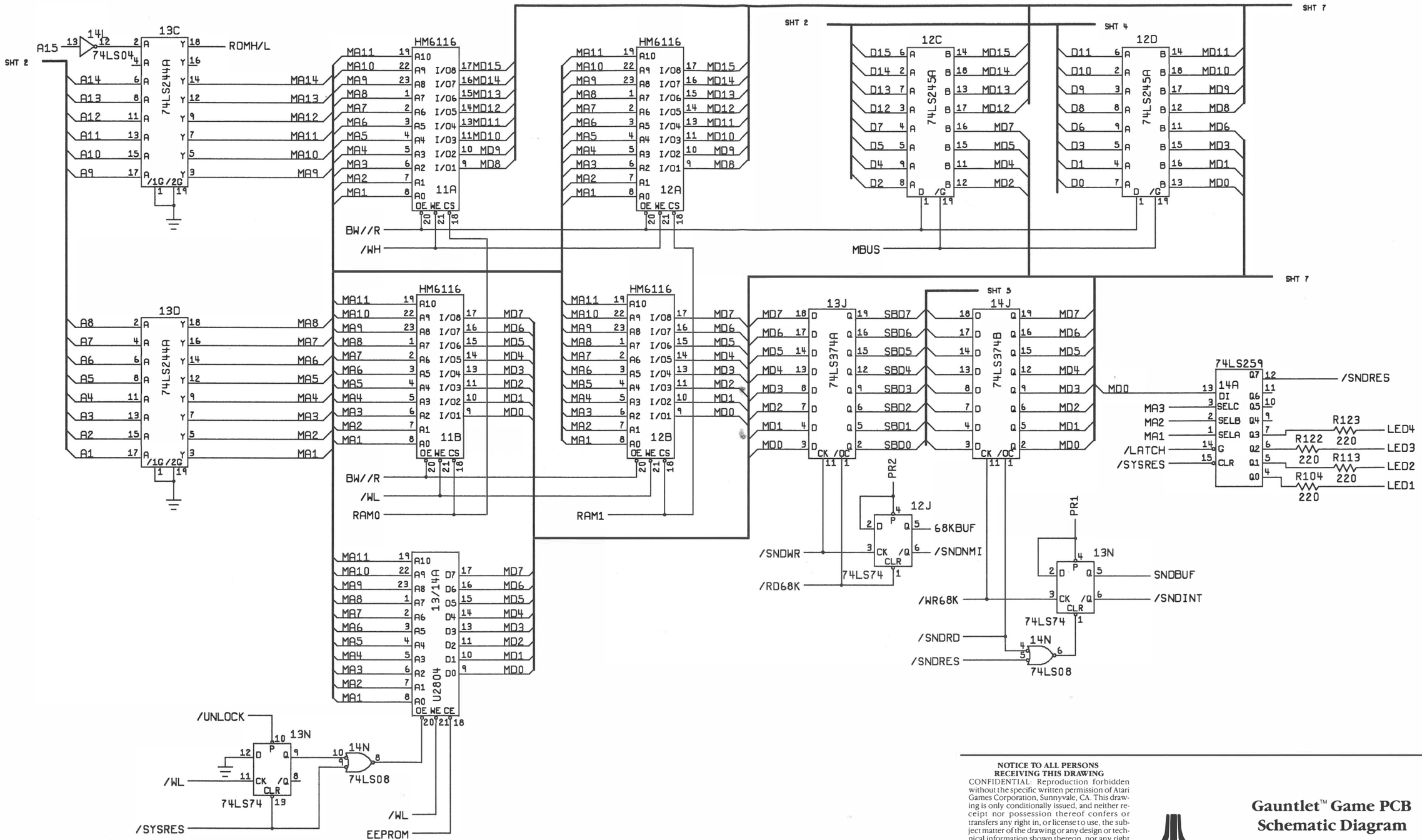
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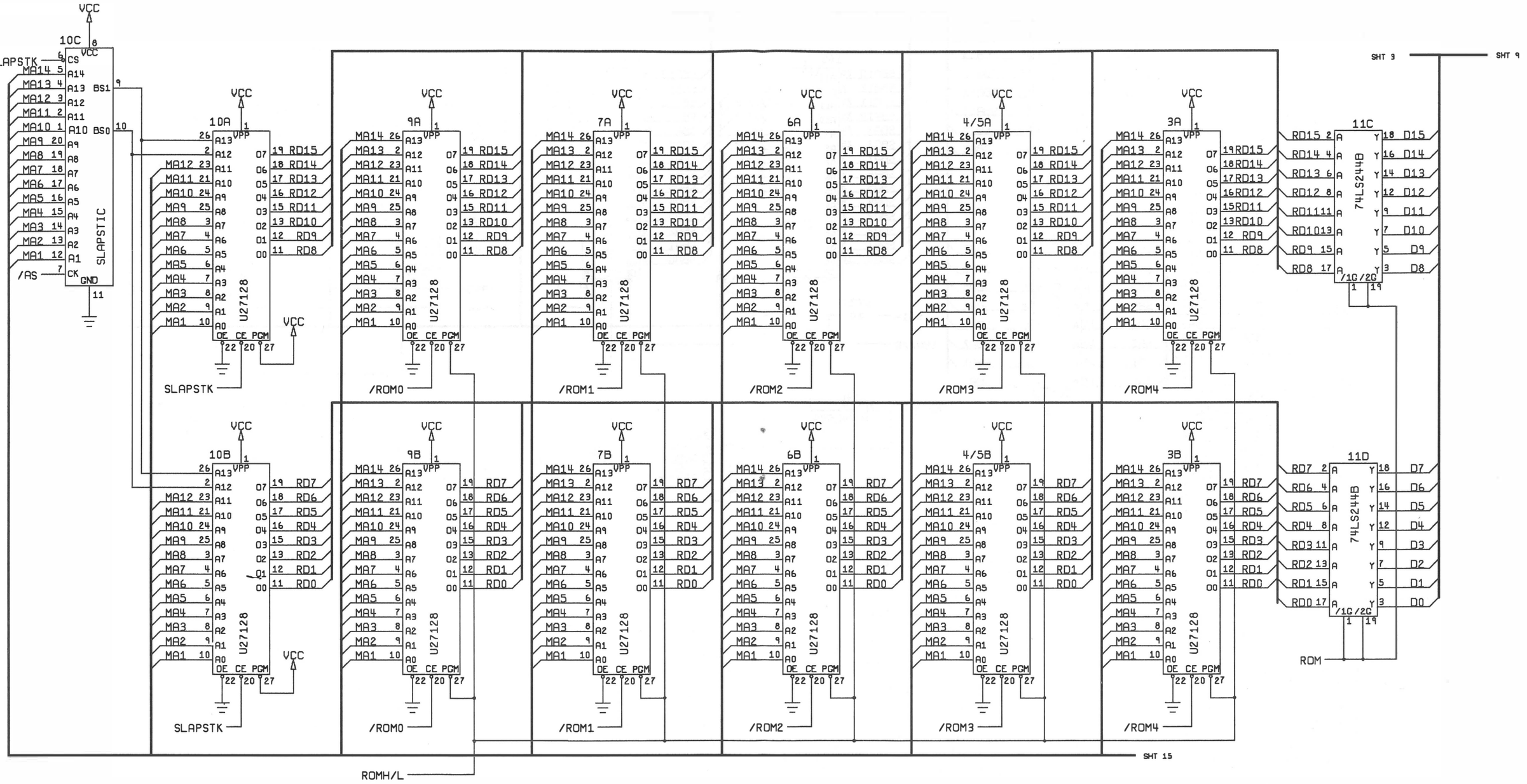
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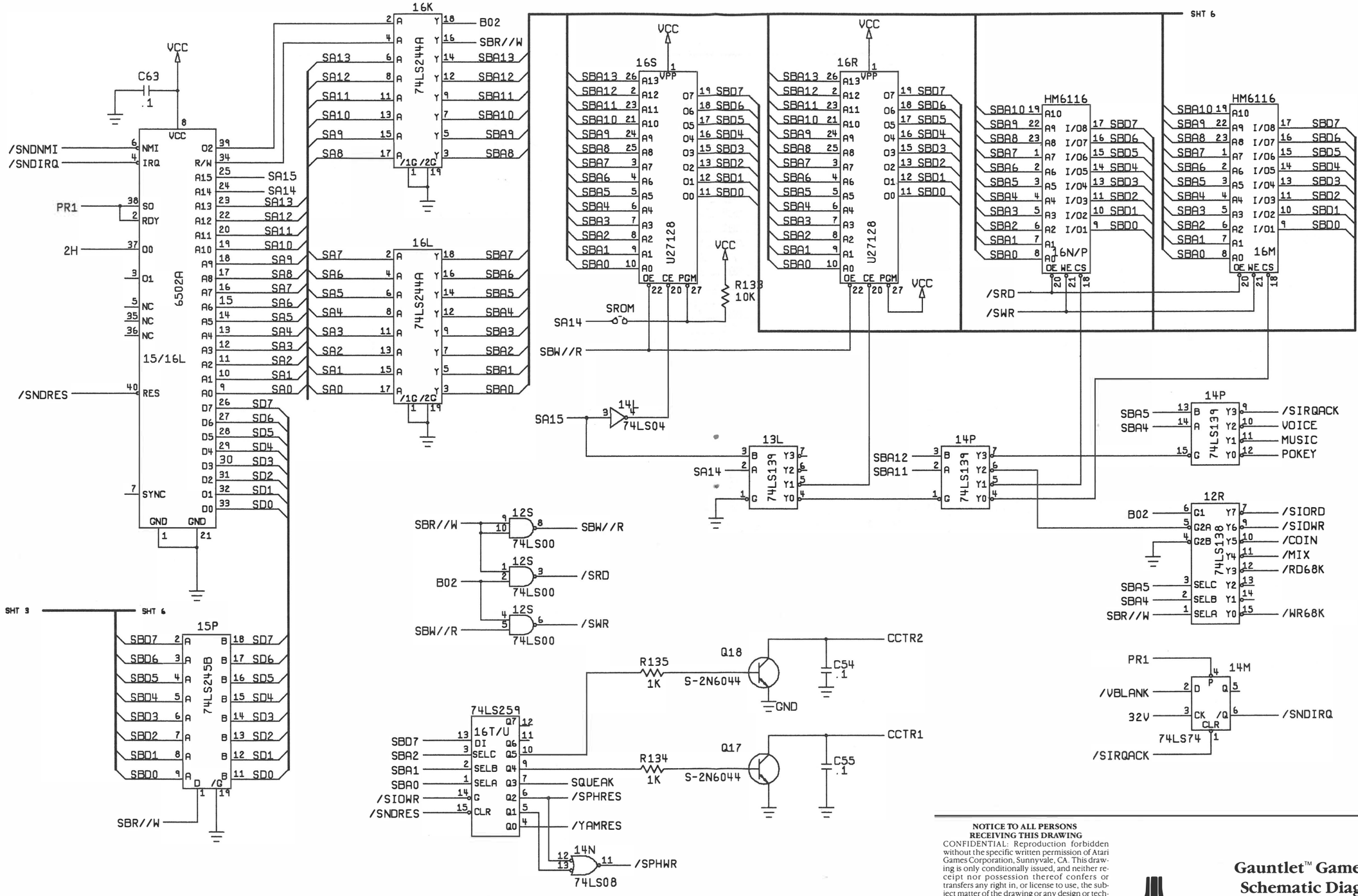
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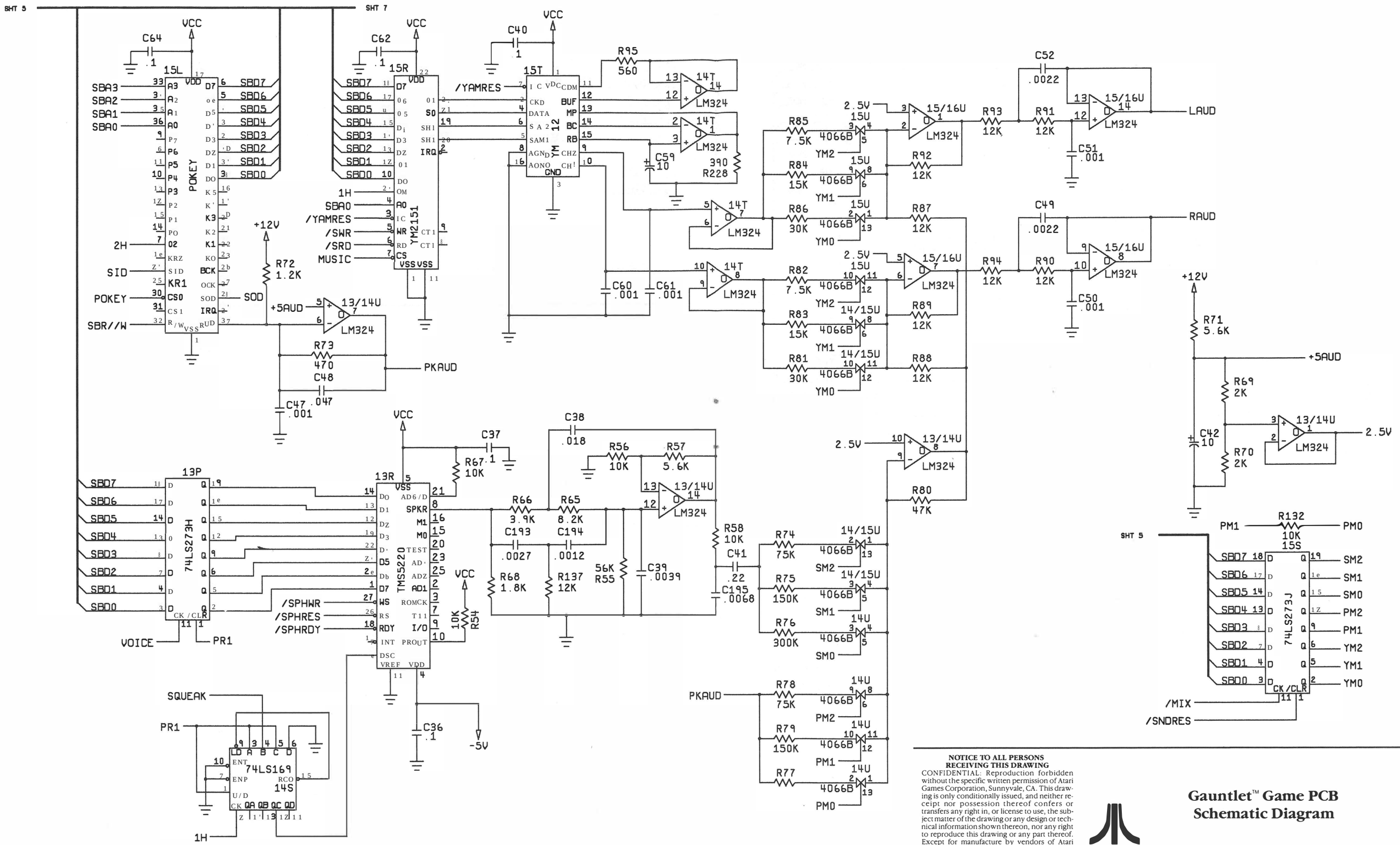
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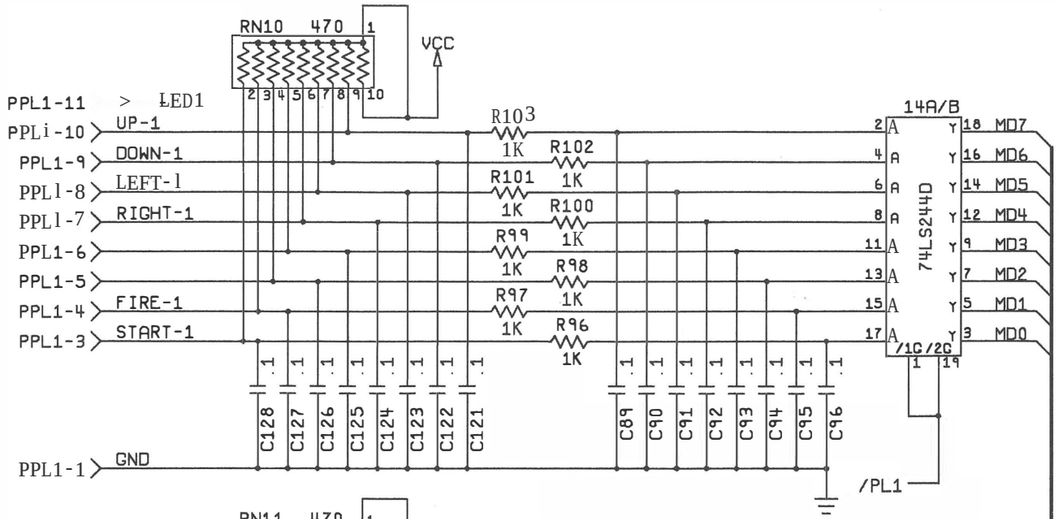
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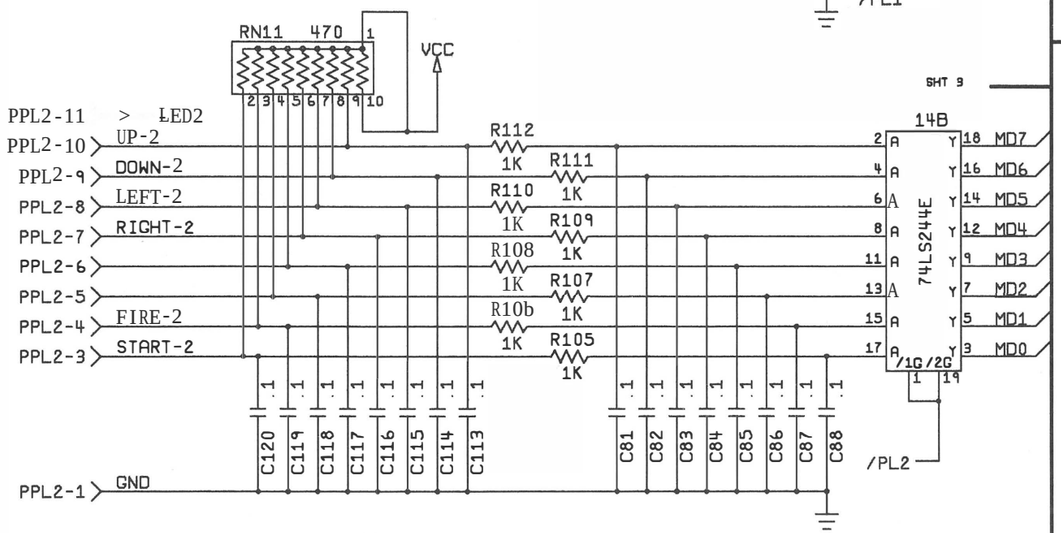
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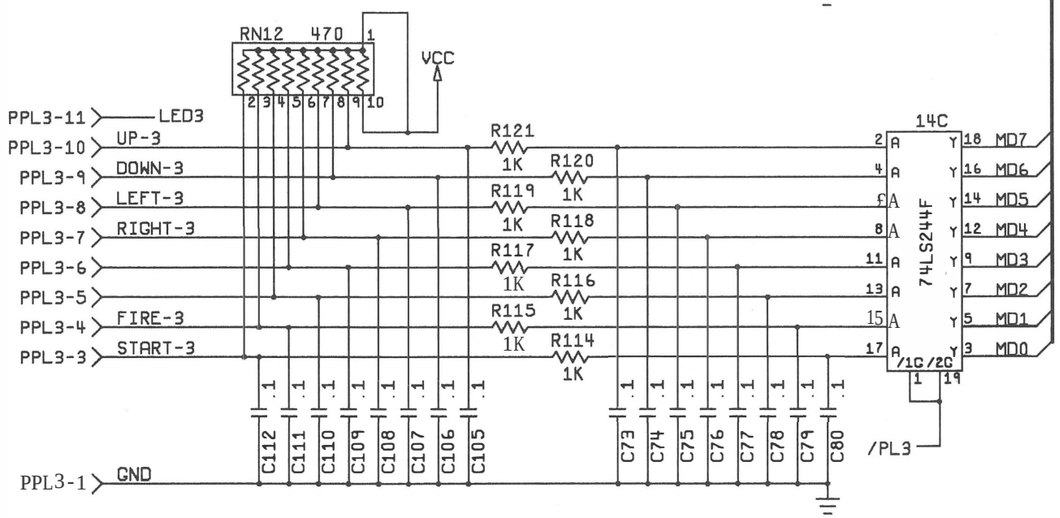
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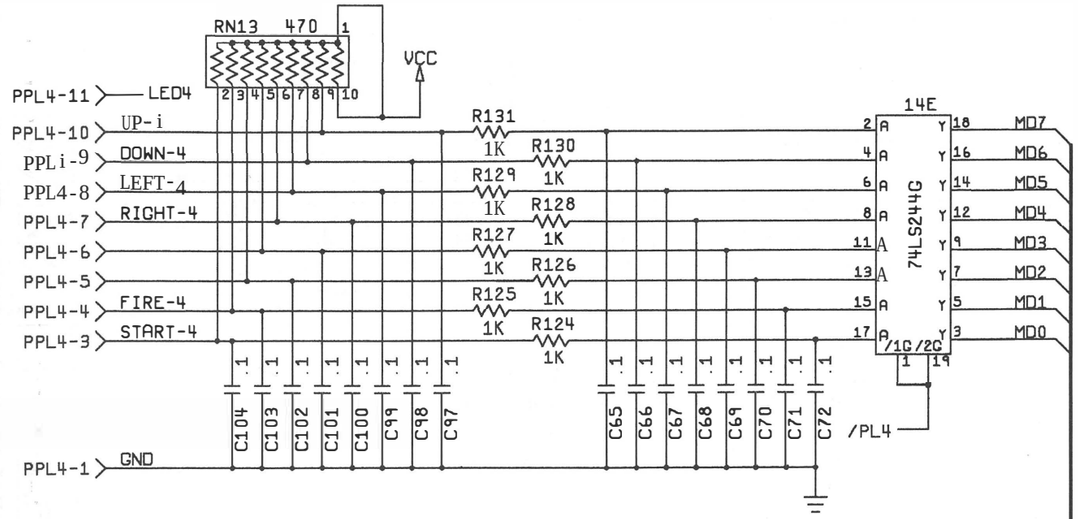
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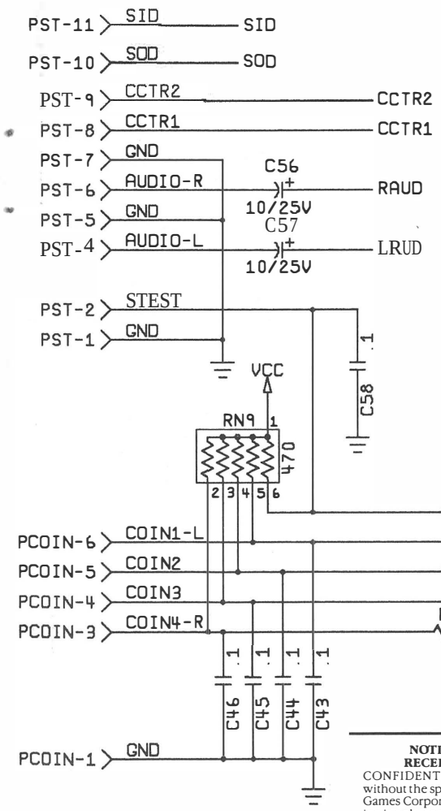
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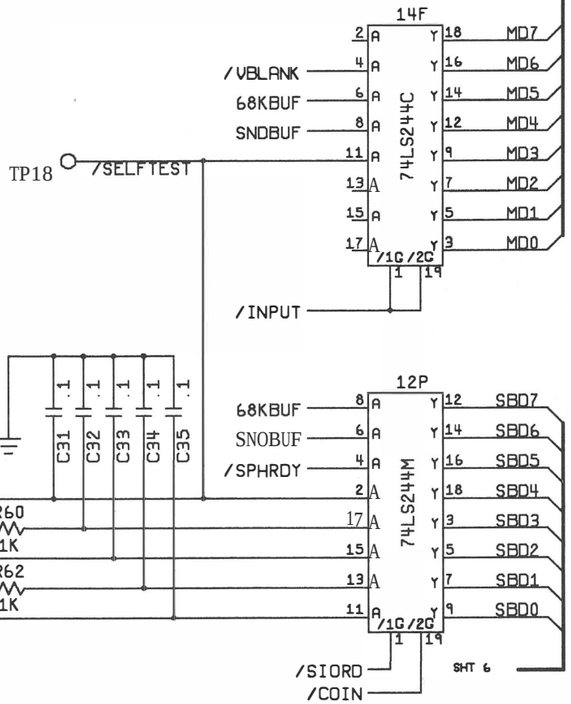












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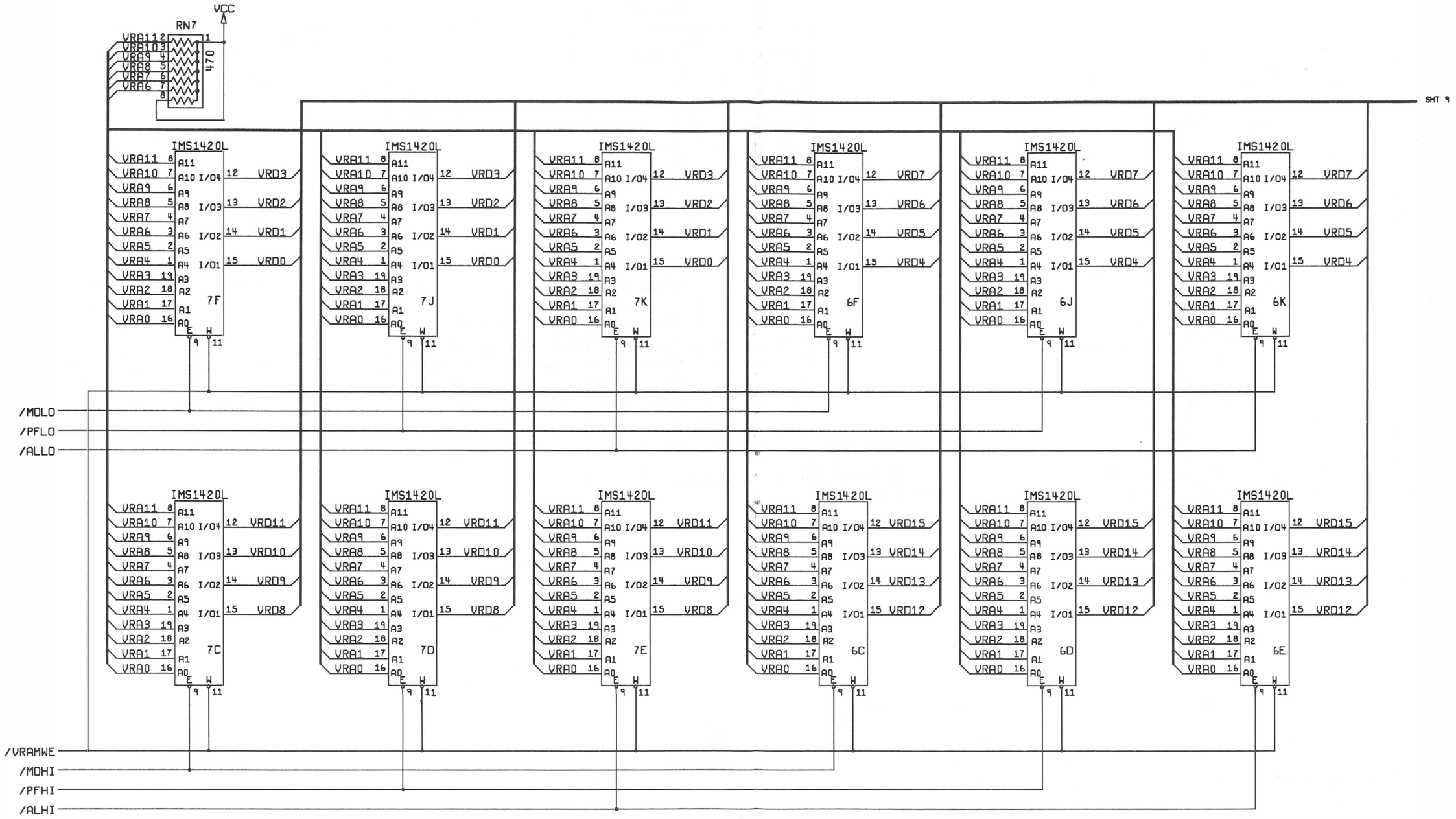
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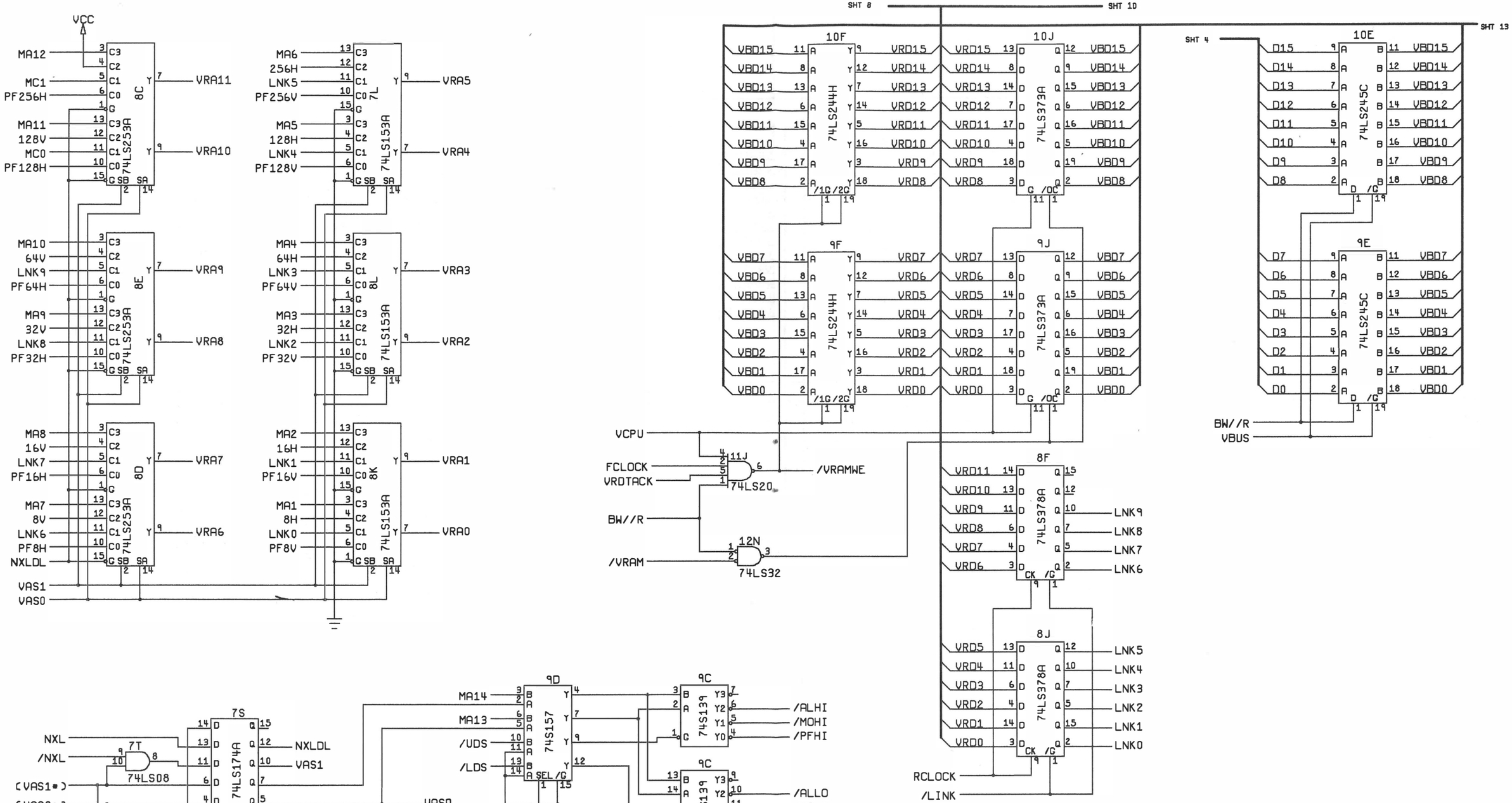
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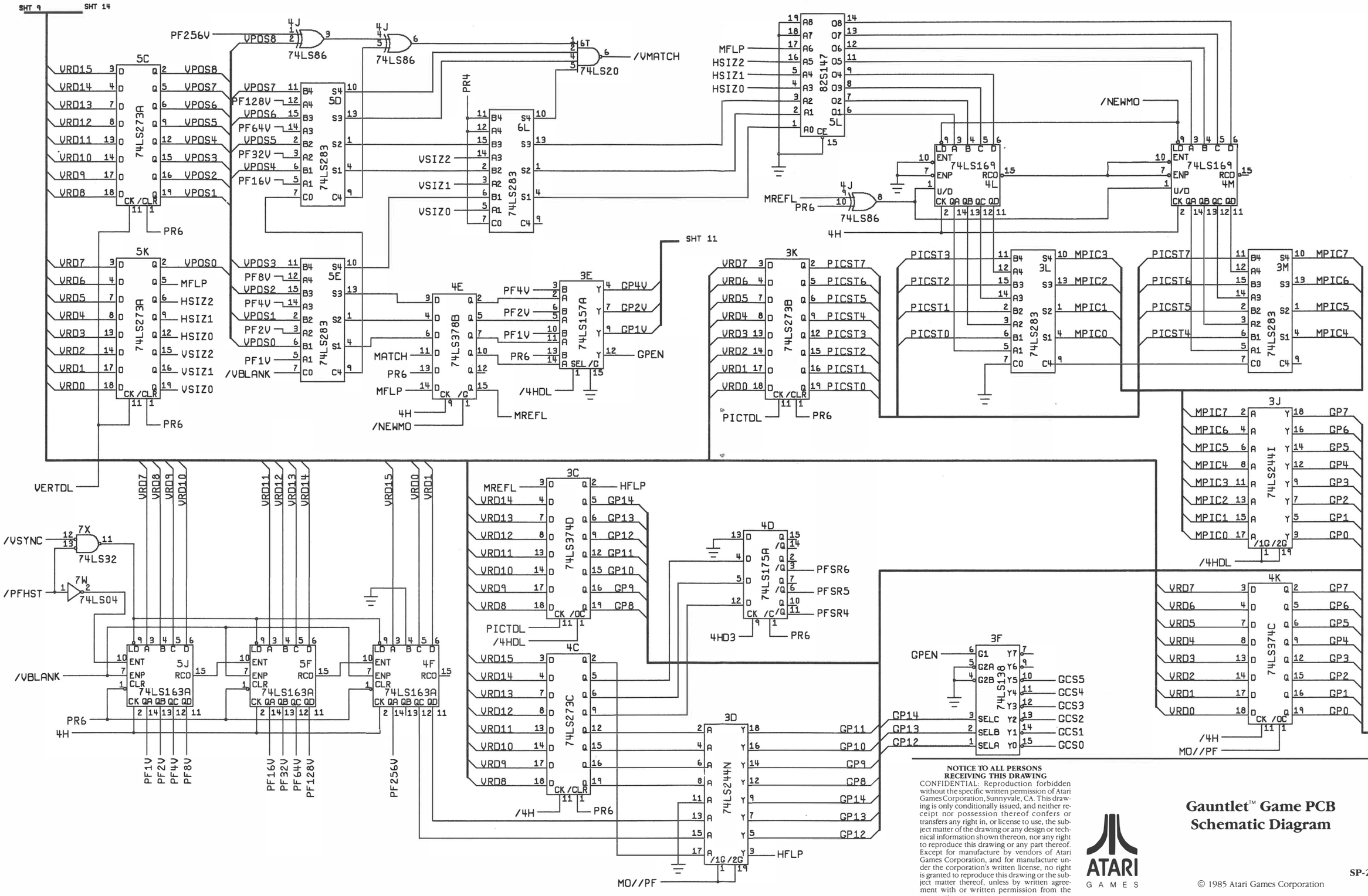
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SHT 10

SHT 12

PLANE 1

PLANE 0

1L 1M/N 1P 1R 1S/T 1U

1A 1B 1C 1D 1E/F 1J

U27128

VCC

RN5 4.7K

RN3 4.7K

C1 .1

1K

SLAGS

HFLP

MO//PF

/GLD

RCLOCK

MOSR1 MOSR0 PFSR1 PFSR0

GCS0 GCS1 GCS2 GCS3 GCS4 GCS5

GRH/L

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SHT 11

PLANE 3

PLANE 2

2L 2M/N 2P 2R 2S/T 2U

2A 2B 2C 2D 2E/F 2J

U27128

VCC

GP10 GP9 GP8 GP7 GP6 GP5 GP4 GP3 GP2 GP1 GP0 GP4V GP2V GP1V

A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

O7 O6 O5 O4 O3 O2 O1 O0

VPP OE CE PGM

RN6 4.7K

RN4 4.7K

C2 .1

2K SLAGS

VDD VSS

HLDB HLDA BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0

MODB MOSR3 PFDB PFSR3 MODA MOSR2 PFDA PFSR2

AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

HFLP MO//PF /GLD RCLOCK

FLP MO/PF LD PHIN

GCS0 GCS1 GCS2 GCS3 GCS4 GCS5

4J 74LS86

GP11 PR6 GRH/L

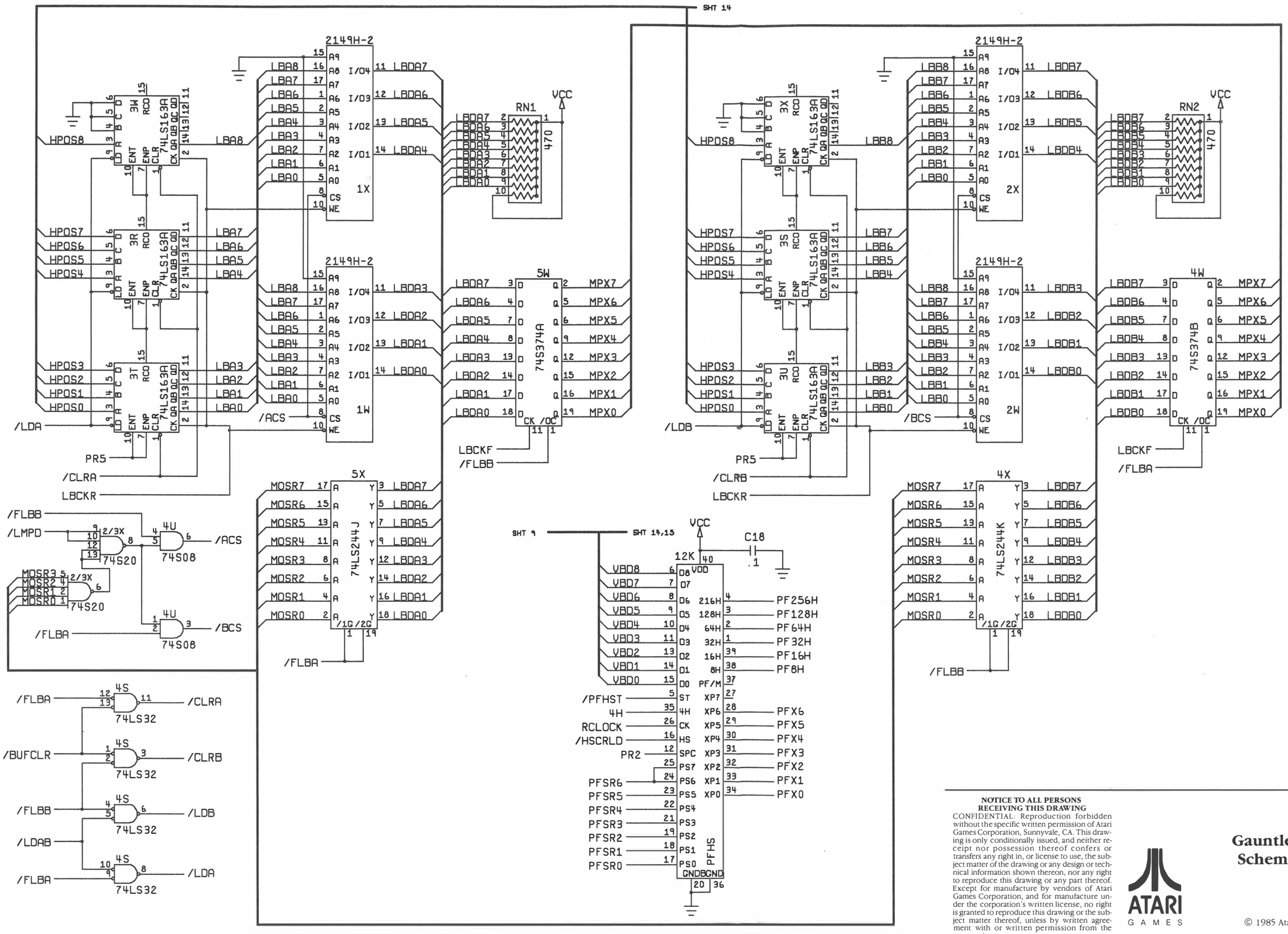
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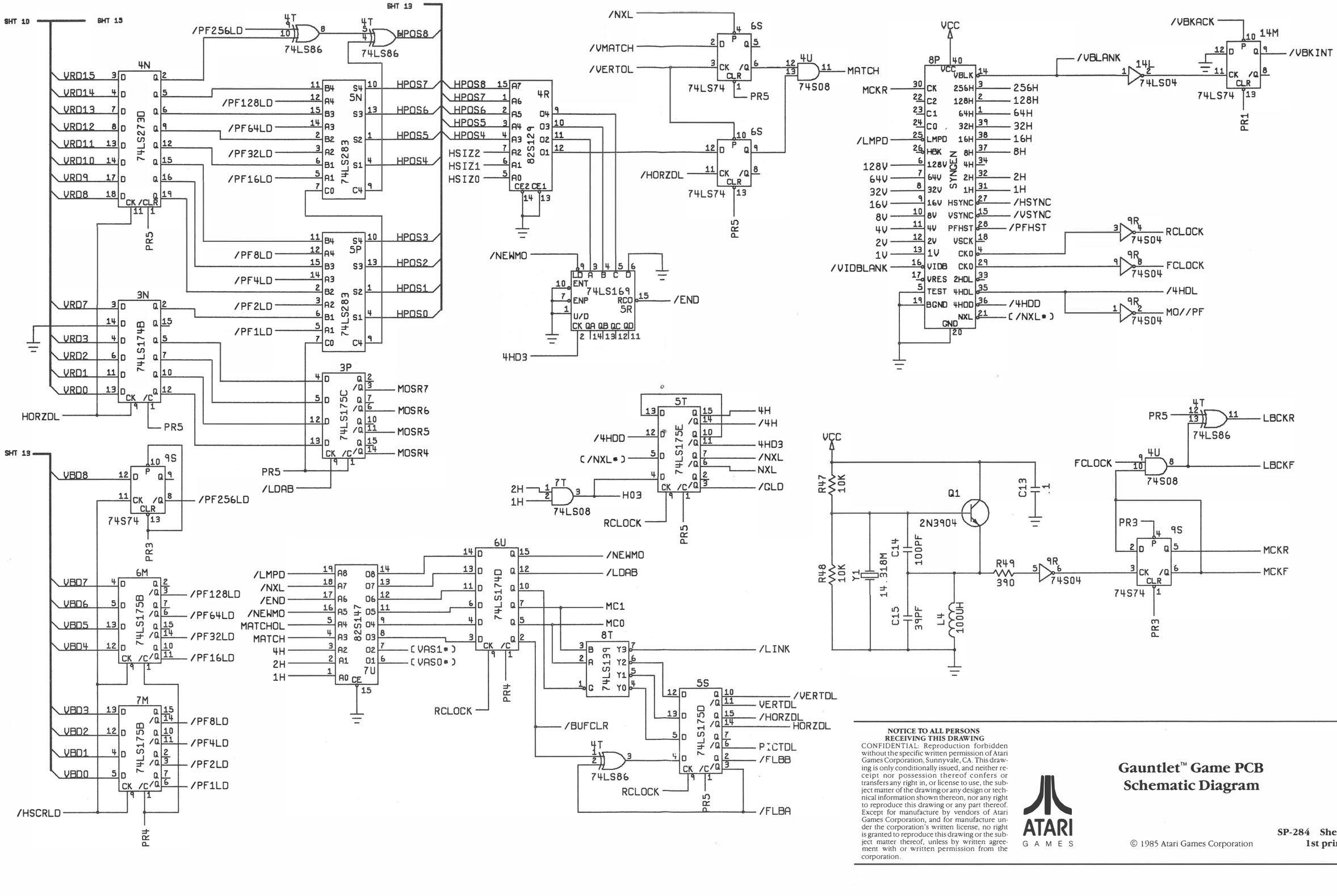
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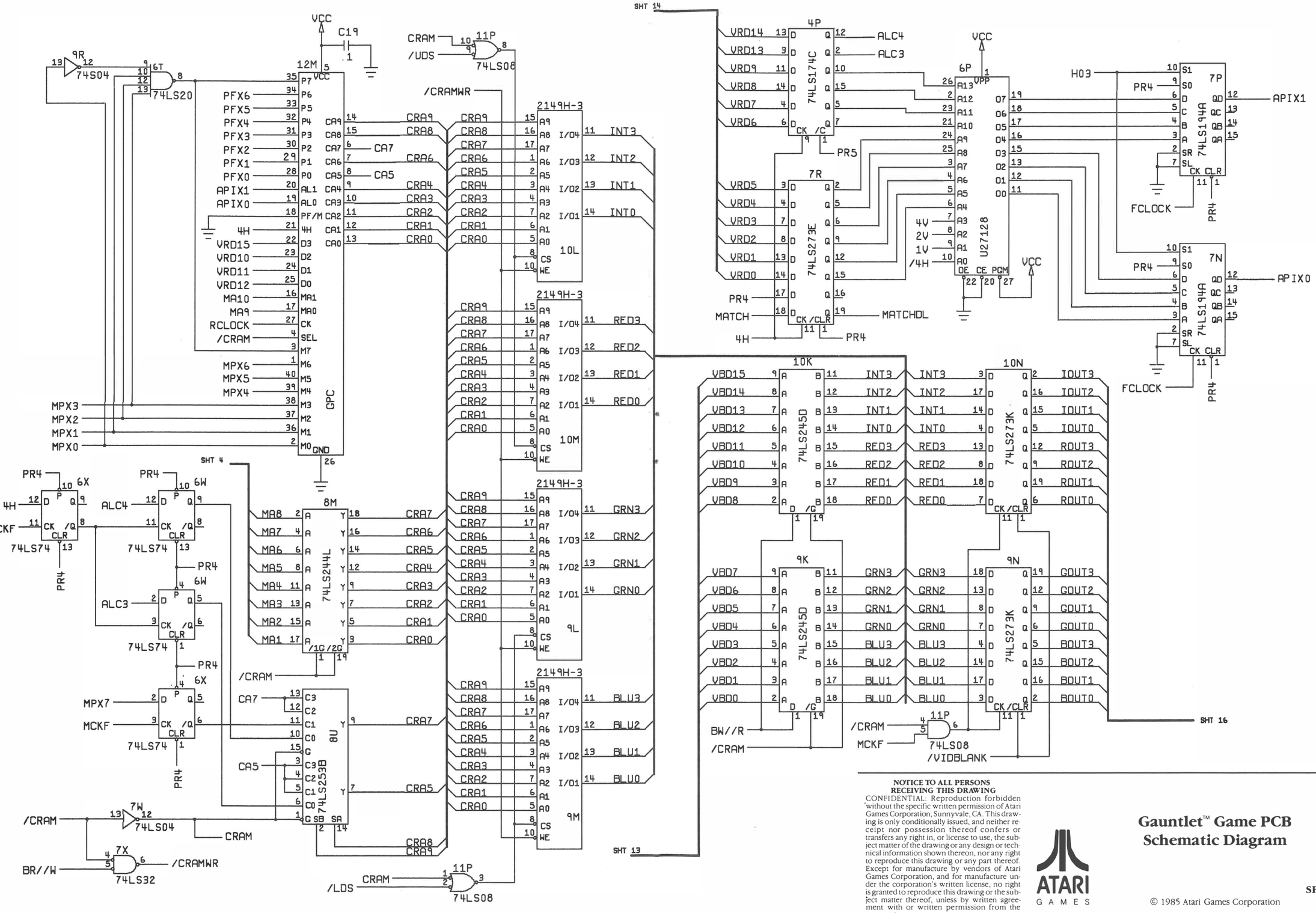
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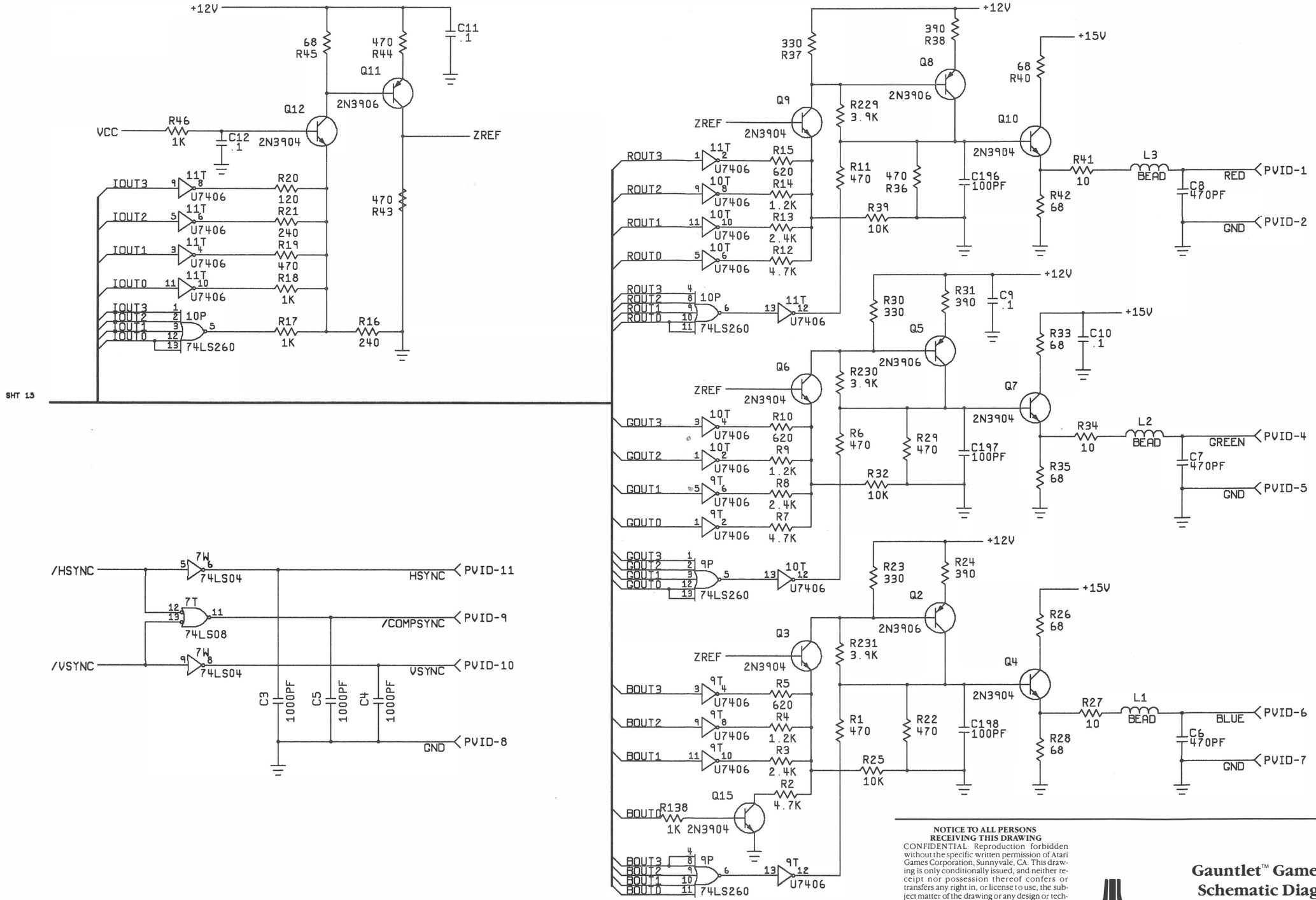
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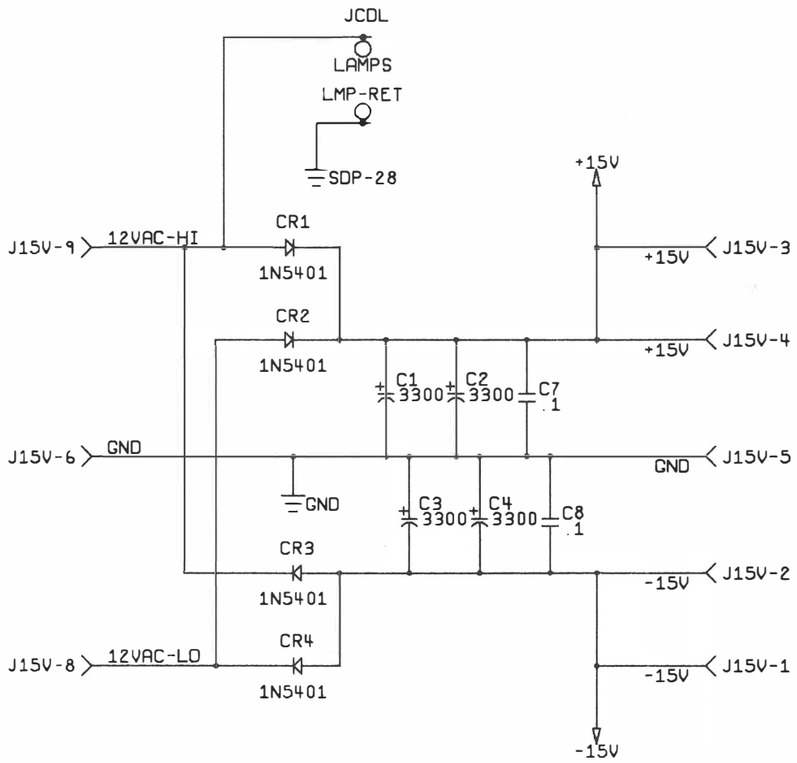
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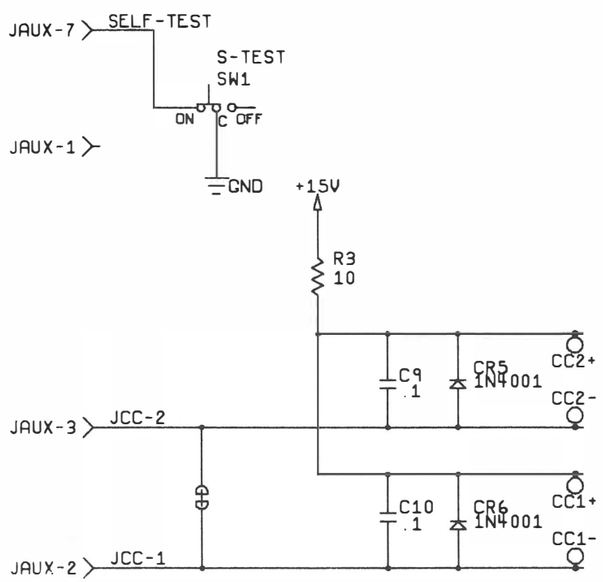
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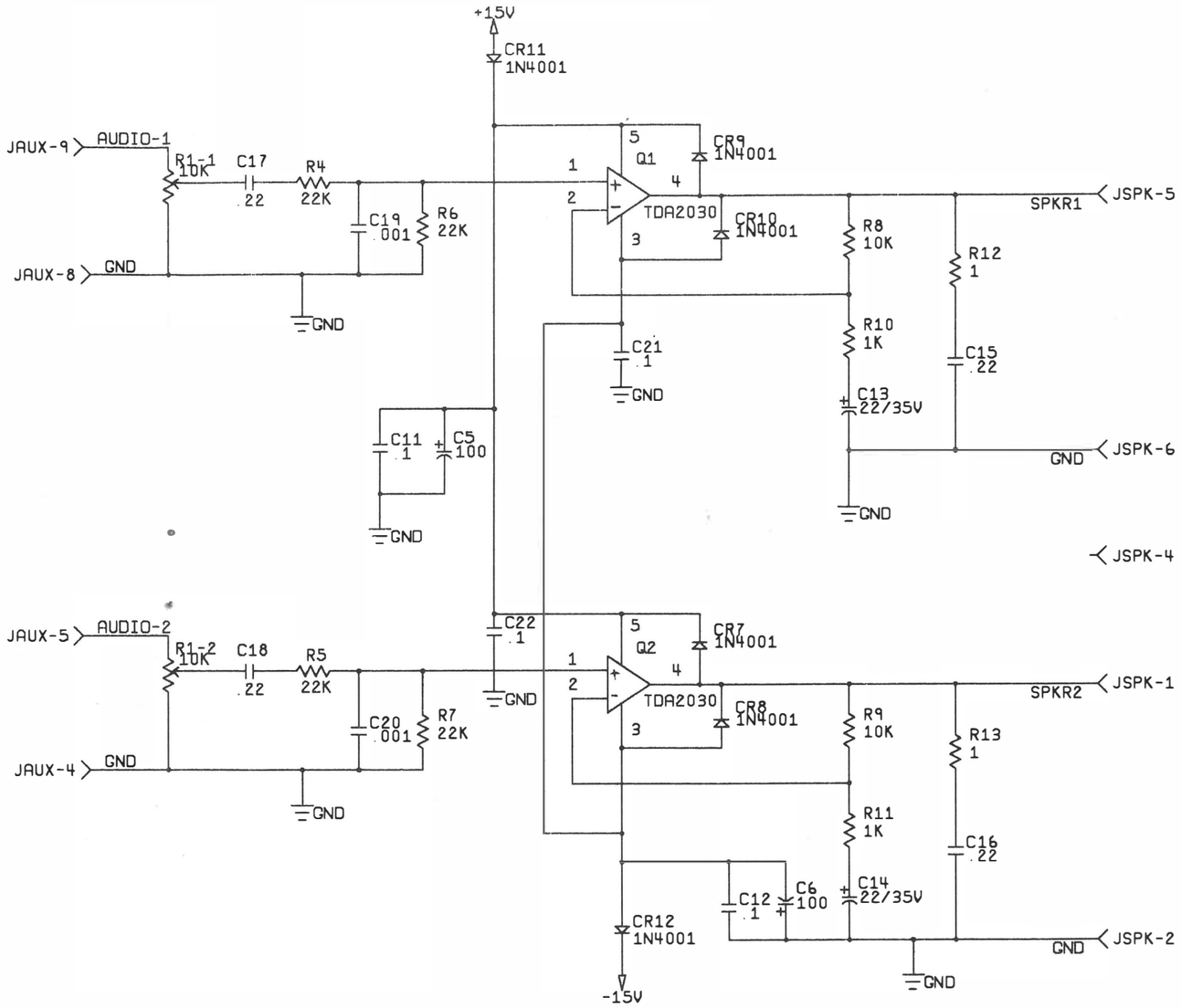
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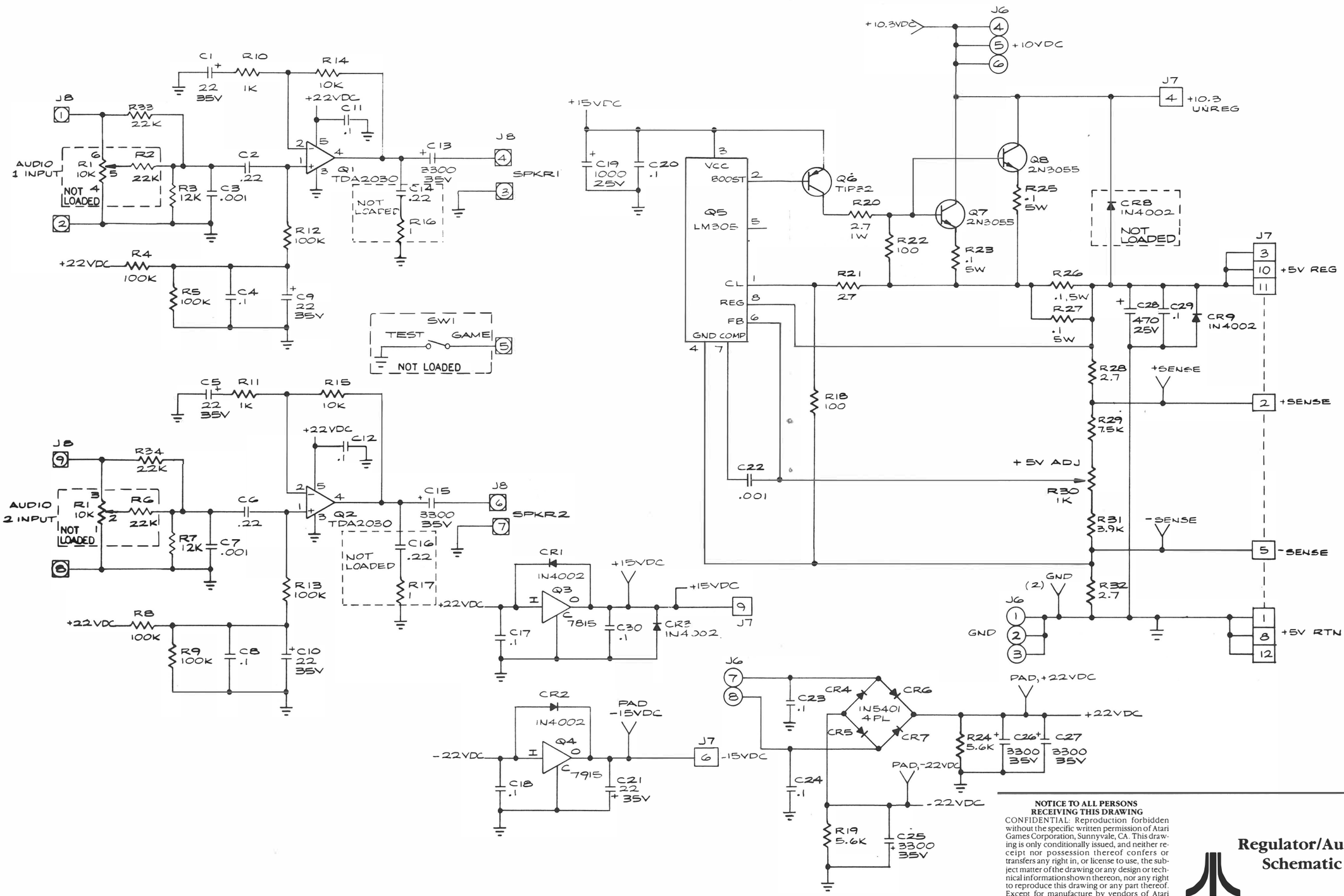
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Audio PCB Assembly Schematic Diagram (U.S.)

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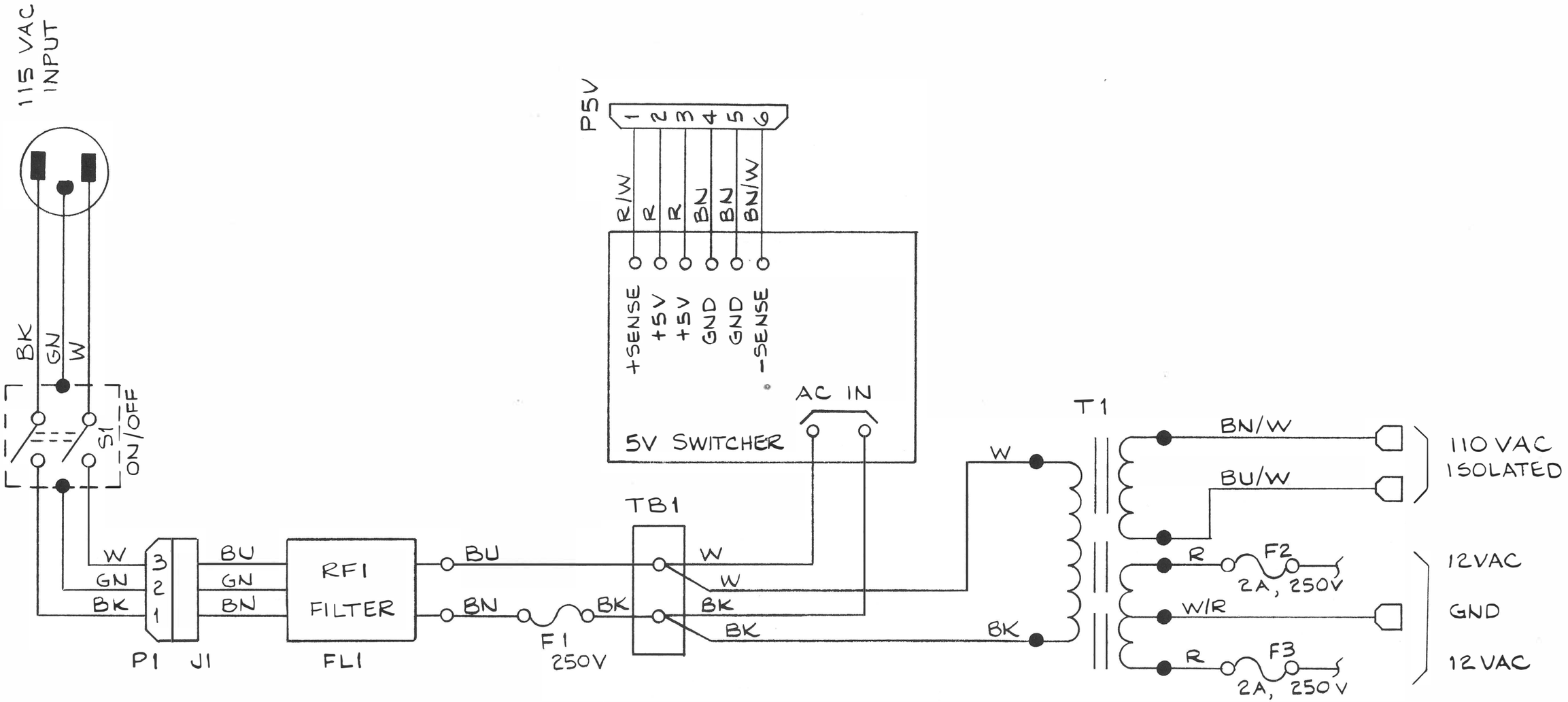
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Regulator/Audio III PCB Assembly Schematic Diagram (Ireland)

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Switching/Linear (SL) Power Supply Wiring Diagram (U.S.)

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GRAY WIRES 200V 9 8 7 6 5 4 3 2 1

BLUE WIRES 220V 9 8 7 6 5 4 3 2 1

BROWN WIRES 240V 9 8 7 6 5 4 3 2 1

VOLTAGE SELECTION BLOCKS

VIOLET WIRES 100V 9 8 7 6 5 4 3 2 1

YELLOW WIRES 120V 9 8 7 6 5 4 3 2 1

J3 9 8 7 6 5 4 3 2 1

W BK W/BK W V/BK BK/Y OR/BK R/BK BN/BK

120V BN/BK

100V R/BK

COM. OR/BK

120V Y/BK

100V V/BK

COM BU/BK

W/BK 110±5°C

T1

MDA3501 OR/BK

27,000µf @15VDC OR/W

CR1 C1

OR OR OR V/W V V V/W

20A,SB 32V 3 F3 OR

OR OR

R R F4 4 A, SB 250V

V/W

4 A, SB 250V F5 R (R/W)

R Y

Y F6 4 A, SB 250V

BN

GY/BN

BN/W

BU

GY/BU

BU/W

4A, SB 250V F2

J5

OR/W	1		10.6 VDC
OR	2		10.6 VDC
OR	3		10.6 VDC
V	4		GND
V	5		GND
R	6		36 VAC CT
R (R/W)	7		
Y	8	KEY	6.1 VAC
Y	9		
BN	10		60 VAC CT
GY/BN	11		
BN/W	12		
BU	13		60 VAC CT
GY/BU	14		
BU/W	15		

5

W BU/BK BK/Y Y/BK

20 01 TBI

J4B 120V AC OUT 3 2 1 W GN BK 4

J4A 120V AC OUT 3 2 1 W GN BK

1 PLUG BN GN/Y BU J1 1 2 3 BN GN/Y BU FL1 AC GND NEUT. AC BN BU F1 7A,SB 250V 2 BN BU BK W GN J2 1 2 3 4 5 6 TO ON/OFF & INTERLOCK SWITCHES

NOTES

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
2. USE 4 AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).
5. ALTERNATE WIRE COLOR IS IN PARENTHESES ( ).

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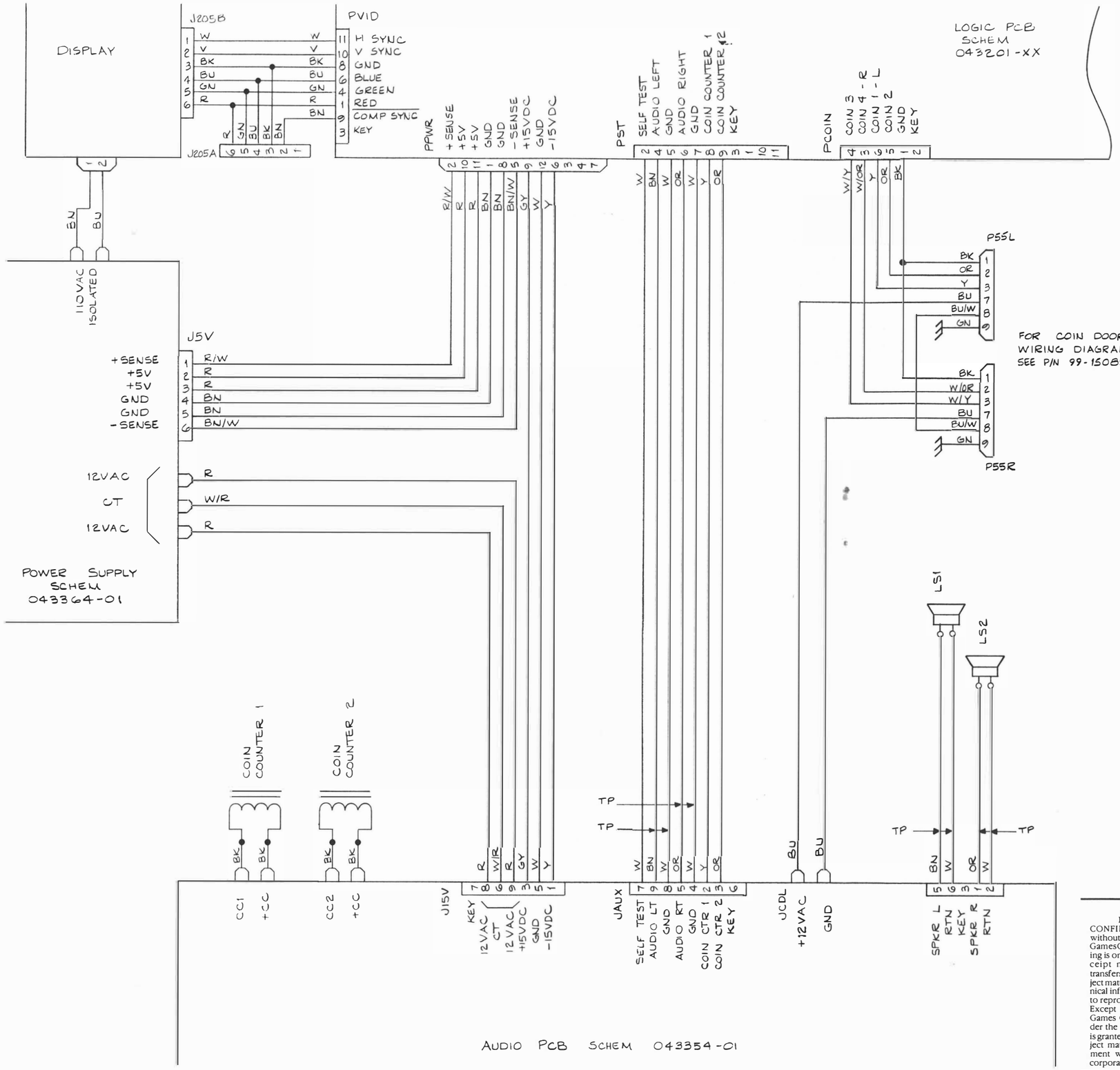
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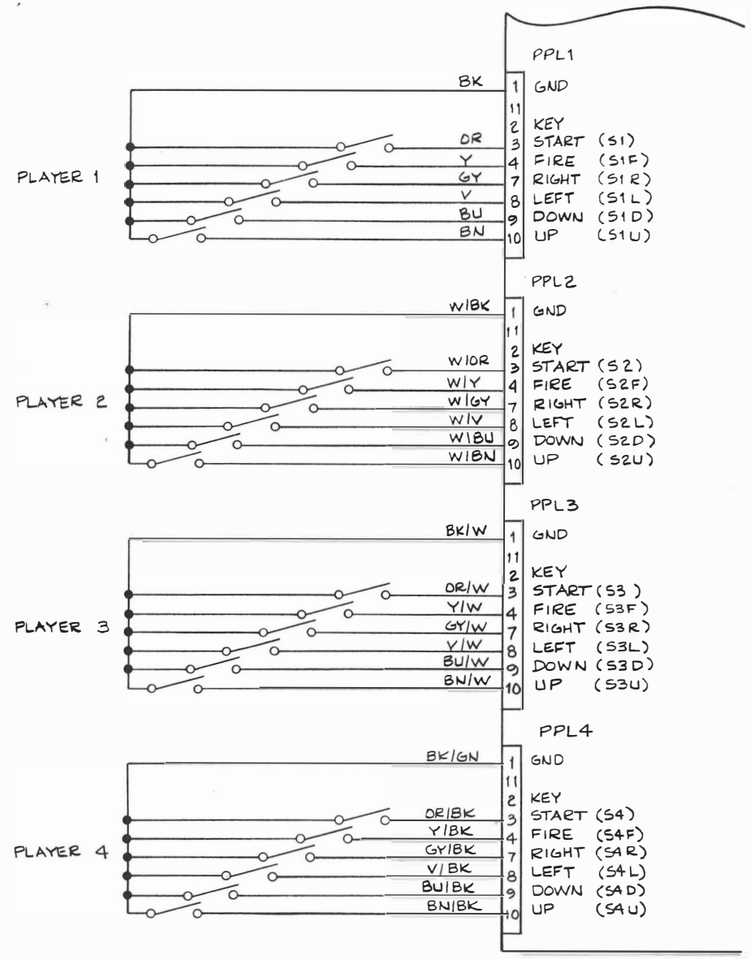
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Linear Power Supply Wiring Diagram (Ireland)

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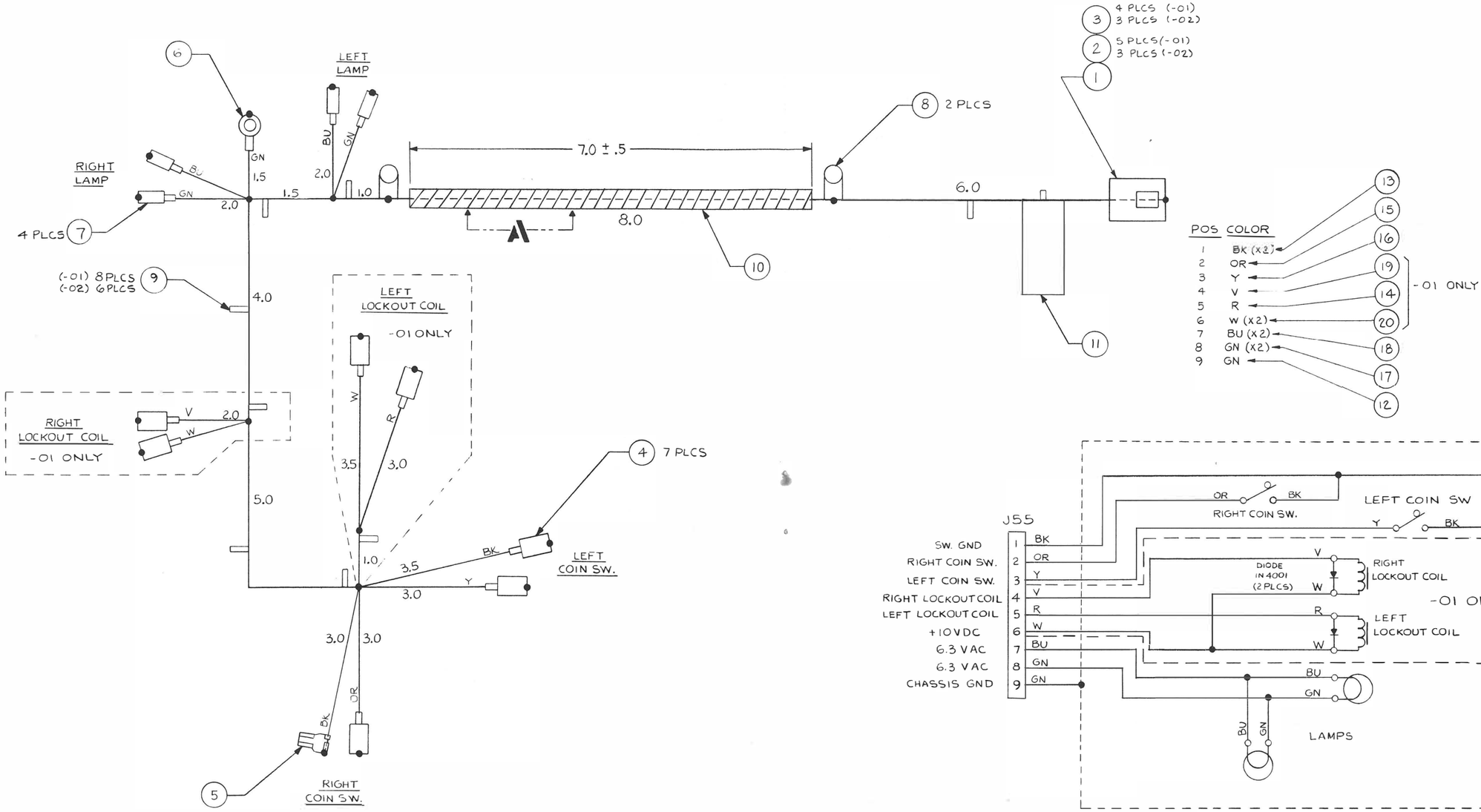
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Gauntlet™ Game Wiring Diagram

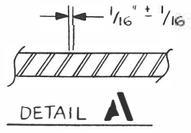
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COIN DOOR WIRING DIAGRAM



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Coin Door Wiring Diagram

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Gauntlet™ 68010 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program ROM/Operating System	000000–00FFFF	R	D0–D15
Program ROM/SLAPSTIC	038000–03FFFF	R	D0–D15
Program ROM/Main	040000–07FFFF	R	D0–D15
Spare RAM	800000–801FFF	R/W	D0–D15
EEPROM	802001–802FFF	R/W	D7–D0
Player 1 Input (see detail below)	803001	R	D0–D71
Player 2 Input	803003	R	D0–D7
Player 3 Input	803005	R	D0–D7
Player 4 Input	803007	R	D0–D7
Player Inputs:			
Joystick Up			D7
Joystick Down			D6
Joystick Left			D5
Joystick Right			D4
Spare			D3
Spare			D2
Fire			D1
Magic/Start			D0
VBLANK (Active Low)	803009	R	D6
Output/Buffer Full (@ 803170) (Active High)	803009	R	D5
Input/Buffer Full (@ 80300F) (Active High)	803009	R	D4
Self-Test (Active Low)	803009	R	D3
Read Sound Processor (6502)	80300F	R	D0–D7
Watchdog (128 msec. timeout)	803100	W	xx
LED-1 (Low On)	803121	W	D0
LED-2 (Low On)	803123	W	D0
LED-3 (Low On)	803125	W	D0
LED-4 (Low On)	803127	W	D0
Sound Processor Reset (Low Reset)	80312F	W	D0
VBlank Acknowledge	803140	W	xx
Unlock EEPROM	803150	W	xx
Write Sound Processor (6502)	803171	W	D0–D7
Playfield RAM	900000–901FFF	R/W	D0–D15
Motion Object Picture	902000–9027FF	R/W	D0–D15
Motion Object Horizontal Position	902800–902FFF	R/W	D0–D15
Motion Object Vertical Position	903000–9037FF	R/W	D0–D15
Motion Object Link	903800–903FFF	R/W	D0–D15
Spare RAM	904000–904FFF	R/W	D0–D15
Alphanumerics RAM	905000–905FFF	R/W	D0–D15
Playfield Vertical Scroll	905F6E, 905F6F	R/W	D7–D15
Playfield ROM Bank Select	905F6F	R/W	D0, D1
Color RAM Alpha	910000–9101FF	R/W	D0–D15
Color RAM Motion Object	910200–9103FF	R/W	D0–D15
Color RAM Playfield Shadow	910400–9104FF	R/W	D0–D15
Color RAM Playfield	910500–9105FF	R/W	D0–D15
Color RAM (Spare)	910600–9107FF	R/W	D0–D15
Playfield Horizontal Scroll	930000, 930001	W	D0–D8

NOTE
All addresses can be accessed in byte or word mode.

Gauntlet™ 6502 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program RAM	0000–0FFF	R/W	D0–D7
Write 68010 Port (Output Buffer)	1000	W	D0–D7
Read 68010 Port (Input Buffer)	1010	R	D0–D7
Audio Mix:			
Speech Mix	1020	W	D5–D7
Effects Mix	1020	W	D3, D4
Music Mix	1020	W	D0–D2
Coin 1 (Left)	1020	R	D3
Coin 2	1020	R	D2
Coin 3	1020	R	D1
Coin 4 (Right)	1020	R	D0
Data Available (@ 1010) (Active High)	1030	R	D7
Output Buffer Full (@ 1000) (Active High)	1030	R	D6
Speech Ready (Active Low)	1030	R	D5
Self-Test (Active Low)	1030	R	D4
Music Reset (Low Reset)	1030	W	D7
Speech Write (Active Low)	1031	W	D7
Speech Reset (Active Low)	1032	W	D7
Speech Squeak (Low = 650KHz Clock)	1033	W	D7
Coin Counter Right (Active High)	1034	W	D7
Coin Counter Left (Active High)	1035	W	D7
Effects	1800–180F	R/W	D0–D7
Music	1810–1811	R/W	D0–D7
Speech	1820	W	D0–D7
Interrupt Acknowledge	1830	R/W	xx
Program ROM (48k bytes)	4000–FFFF	R	D0–D7

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Gauntlet™ 68010 and 6502 Microprocessor Memory Maps

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Gauntlet Signal Name Glossary

2.5V	2.5 volts audio amplifier reference
+5AUD	5 volts audio amplifier reference
10.3V	Power-on-reset control voltage
+12V	+12 volts regulated
+15V	+15 volts unregulated
−15V	−15 volts unregulated
−5V	−5 volts regulated
1H–256H	Screen horizontal address counter chain
1V–128V	Screen vertical address counter chain
$\overline{4H}$	Inverted 4H signal
4HD3, $\overline{4HD3}$	4H signal delayed three clock cycles
$\overline{4HDD}$	4H signal delayed two clock cycles
$\overline{4HDL}$	4H signal delayed one clock cycle
68KBUF	68010 output buffer full (to 6502)
A1–A23	68010 address bus unbuffered
$\overline{ACS}$	"A" line buffer RAMs chip select
ALC3, ALC4	Alphanumerics palette data bits 3 and 4
$\overline{ALHI}$, $\overline{ALLO}$	Alphanumerics RAM chip selects
APIX0, APIX1	Alphanumerics pixel data
$\overline{AS}$	68010 address strobe
AUDIO-L, AUDIO-R	Left and right audio outputs (5V peak-to-peak)
B02	6502 buffered phase 2 (Φ2)
BAS	Buffered address strobe (see $\overline{AS}$)
$\overline{BCS}$	"B" line buffer RAMs chip select
BLU0–BLU3	Blue color RAM data
BLUE	Blue analog video output
BOUT0–BOUT3	Blue latched digital video output
BR/$\overline{W}$	68010 read/write control, buffered
$\overline{BUFCLR}$	Swap "A" and "B" line buffers, clear line buffer counter chain
BW/$\overline{R}$	68010 read/write inverted, buffered
CA5, CA7	Color RAM address bits 5 and 7
CCTR1, CCTR2	Coin counter outputs 1 and 2
$\overline{CLRA}$	Clear line buffer "A" address counters
$\overline{CLRB}$	Clear line buffer "B" address counters
$\overline{COIN}$	Coin input buffer chip select
COIN1-L, COIN2, COIN3, COIN4-R	Four coin switch inputs
$\overline{COMPSYNC}$	Negative composite sync output
CRA0–CRA9	Color RAM address
$\overline{CRAM}$, CRAM	68010 address decode for color RAM
$\overline{CRAMWR}$	Color RAM write enable
D0–D15	68010 data bus, unbuffered
DOWN-1–DOWN-4	Joystick down switch inputs, players 1–4
EEPROM	Electrically erasable PROM chip select
$\overline{END}$	Current motion object finished
FCLOCK	System clock inverted phase
FIRE-1–FIRE-4	Fire switch inputs, players 1–4
$\overline{FLBA}$	Line buffer "A" fill control
$\overline{FLBB}$	Line buffer "B" fill control
GCS0–GCS5	Graphics ROMs chip select
$\overline{GLD}$	Graphics load (to SLAGS chips)
GND	System ground
GOUT0–GOUT3	Green latched digital video output
GP0–GP14	Graphics picture address
GP1V, GP2V, GP4V	Graphics picture stamp sub-address
GPEN	Graphics picture enable
GREEN	Green analog video output
GRH/L	Graphics ROM high/low select (A14 on a 27256)
GRN0–GRN3	Green color RAM data
H03	Alphanumerics load (to shift registers)
HFLP	Graphics stamp horizontal flip
$\overline{HORZ}$	Latch motion object horizontal data and palette data
HORZDL, $\overline{HORZDL}$	HORZ delayed one clock cycle
HPOS0–HPOS8	Motion object horizontal position data
$\overline{HSCRLD}$	Latch playfield horizontal scroll data

Gauntlet Signal Name Glossary, continued

HSIZ0–HSIZ2	Motion object horizontal size
HSYNC, $\overline{HSYNC}$	Horizontal sync output
$\overline{INPUT}$	68010 miscellaneous inputs buffer select
INT0–INT3	Color intensity RAM data
IOUT0–IOUT3	Intensity latched digital video output
$\overline{LATCH}$	68010 miscellaneous latched outputs chip select
LAUD	Summed left channel audio
LBA0–LBA8	Line buffer "A" address bus
LBB0–LBB8	Line buffer "B" address bus
LBCKF	Line buffer clock inverted phase
LBCKR	Line buffer clock
LBDA0–LBDA7	Line buffer "A" data bus
LBDB0–LBDB7	Line buffer "B" data bus
$\overline{LDA}$	Load line buffer "A" address counters
$\overline{LDAB}$	Load line buffer "A" or "B" address counters
$\overline{LDB}$	Load line buffer "B" address counters
$\overline{LDS}$	68010 lower data strobe
LED1–LED4	LED outputs, players 1–4
LEFT-1–LEFT-4	Joystick left switch inputs, players 1–4
$\overline{LINK}$	Latch motion object link data
$\overline{LMPD}$	Stop motion object processing for line buffer changeover
LNK0–LNK9	Motion object link data
MA1–MA14	68010 address bus buffered
MATCH	Motion object H and V data matches current playfield position
MATCHDL	Previous MATCH state
MBUS	68010 "M" data bus buffers enable
MC0, MC1	Motion object parameter control select
$\overline{MCEN}$	Motion object parameter control enable
MCKF	Master clock, inverted phase
MCKR	Master clock
MD0–MD15	68010 "M" data bus
MFLP	Motion object horizontal flip parameter
$\overline{MIX}$	Latch audio mix data
MO/$\overline{PF}$	Motion object or playfield picture select
$\overline{MOHI}$, $\overline{MOLO}$	Motion object RAM chip selects
MOSR0–MOSR3	Motion object pixel data, before the line buffers
MOSR4–MOSR7	Motion object pixel palette data, before the line buffers
MPIC0–MPIC7	The lower 8 bits of the motion object picture address
MPX0–MPX7	Motion object pixel data, after the line buffers
MREFL	Motion object stamp horizontal flip state
MUSIC	Music chip select
$\overline{NEWMO}$	Start a new motion object
NXL, $\overline{NXL}$	Next line
($\overline{NXL*}$)	NXL one clock cycle early
NXLDL	NXL delayed one clock cycle
$\overline{PF1LD–PF256LD}$	Latched playfield horizontal scroll data
PF1V–PF256V	Playfield vertical address counter chain
PF8H–PF256H	Playfield horizontal address counter chain
PFBANK0, PFBANK1	Playfield picture bank select
$\overline{PFHI}$, $\overline{PFLO}$	Playfield RAM chip selects
$\overline{PFHST}$	Playfield scroll control
PFSR0–PFSR3	Playfield pixel data, before PFHS
PFSR4–PFSR6	Playfield pixel palette data, before PFHS
PFX0–PFX6	Playfield pixel data after PFHS
PICST0–PICST7	Motion object picture start address
$\overline{PICT}$	Latch motion object picture data
PICTDL	PICT delayed one clock cycle
PKAUD	Effects chip audio
$\overline{PL1}$–$\overline{PL4}$	Player input chip selects, players 1–4
PM0–PM2	Effects audio mix control bits
POKEY	Effects chip select
PR1–PR6	Pull-up resistors
R/$\overline{W}$	68010 read/write control, unbuffered

NOTE

In this signal name glossary all active-low signals are overscored, e.g., $\overline{COMPSYNC}$. In the schematics printed on Sheets 1–16 a slash (/) in front of a signal name indicates an active-low signal.

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Gauntlet™ Signal Name Glossary

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Gauntlet Signal Name Glossary, continued

RAM0, RAM1	68010 working RAM chip selects
RAUD	Summed right channel audio
RCLOCK	System clock
RD0–RD15	68010 ROM data bus
$\overline{\text{RD68K}}$	6502 read 68010 output buffer
RED	Red analog video output
RED0–RED3	Red color RAM data
RIGHT-1–RIGHT-4	Joystick right switch inputs, players 1–4
ROM	68010 ROM data bus enable
$\overline{\text{ROM0}}$–$\overline{\text{ROM4}}$	68010 program ROM chip selects
ROMH/L	68010 program ROM high/low select (A14 on a 27256)
ROUT0–ROUT3	Red latched digital video output
SA0–SA15	6502 address bus unbuffered
SBA0–SBA13	6502 buffered address bus
SBD0–SBD7	6502 buffered data bus
SBR/$\overline{\text{W}}$	6502 buffered read/write control
SBW/$\overline{\text{R}}$	6502 buffered read/write control inverted
SD0–SD7	6502 data bus unbuffered
$\overline{\text{SELFTEST}}$	Self-test switch input test pad
SID	Serial input data
$\overline{\text{SIORD}}$	6502 miscellaneous input read control
$\overline{\text{SIOWR}}$	6502 output latch control
$\overline{\text{SIRQACK}}$	6502 interrupt acknowledge
SLAPSTK	SLAPSTIC chip select
SM0–SM2	Speech audio mix control bits
SNDBUF	6502 output buffer full (to 68010)
$\overline{\text{SNDINT}}$	68010 interrupt from 6502
$\overline{\text{SNDIRQ}}$	6502 4-millisecond interrupt
$\overline{\text{SNDNMI}}$	6502 non-maskable interrupt
$\overline{\text{SNDRD}}$	68010 read buffer from 6502
$\overline{\text{SNDRES}}$	6502 master reset (controlled by 68010)
$\overline{\text{SNDWR}}$	68010 write to output buffer (to 6502)
SOD	Serial output data
$\overline{\text{SPHRDY}}$	Speech chip ready
$\overline{\text{SPHRES}}$	Speech chip reset
$\overline{\text{SPHWR}}$	Speech chip write
SQUEAK	Speech chip operating frequency control
$\overline{\text{SRD}}$	6502 read phase
START-1–START-4	Start switch inputs, players 1–4
STEST	Self-test switch input
$\overline{\text{SWR}}$	6502 write phase
$\overline{\text{SYSRES}}$	System reset (power up)
$\overline{\text{UDS}}$	68010 upper data strobe
$\overline{\text{UNLOCK}}$	EEPROM write enable control
UP-1–UP-4	Joystick up switch inputs, players 1–4
VAS0, VAS1	Video RAM address control
(VAS0*), (VAS1*)	VAS0 and VAS1 before being latched
VBD0–VBD15	Video RAM buffered data bus
$\overline{\text{VBKACK}}$	Vertical blank interrupt acknowledge
$\overline{\text{VBKINT}}$	Vertical blank interrupt
$\overline{\text{VBLANK}}$	Vertical blank

Gauntlet Signal Name Glossary, continued

VBUS	68010 "V" bus enable (for video RAM)
VCC	System V_{CC} (5 volts regulated)
VCPU	68010-to-video-RAM synchronization control
$\overline{\text{VERT}}$	Latch motion object vertical data and size data
VERTDL, $\overline{\text{VERTDL}}$	VERT delayed one clock cycle
$\overline{\text{VIDBLANK}}$	Video blank (horizontal and vertical blank mixed)
$\overline{\text{VMATCH}}$	Motion object vertical parameter matches current playfield vertical position
VOICE	Speech chip select
VPOS0–VPOS8	Motion object vertical position data
VRA0–VRA11	Video RAM address bus
$\overline{\text{VRAM}}$	68010 address decode for video RAM
$\overline{\text{VRAMRD}}$	68010 read from video RAM
$\overline{\text{VRAMWE}}$	68010 write to video RAM
VRD0–VRD15	Video RAM data bus, unbuffered
VRDTACK	Video RAM to 68010 data acknowledge
VSIZ0–VSIZ2	Motion object vertical size parameter
VSYNC, $\overline{\text{VSYNC}}$	Vertical sync
$\overline{\text{WDOG}}$	Watchdog control
$\overline{\text{WH}}$	68010 write high byte
$\overline{\text{WL}}$	68010 write low byte
$\overline{\text{WR68K}}$	6502 write to output buffer (to 68010)
$\overline{\text{YAMRES}}$	Music chip reset
YM0–YM2	Music audio mix control bits
ZREF	Intensity reference for video output

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Gauntlet™ Signal Name Glossary, Continued

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